Lecture

ACTIVE PIXEL SENSOR (APS) DESIGN- FROM PIXELS TO SYSTEMS

Orly Yadid-Pecht

Abstract: Since active pixel sensors (APS) are fabricated in a commonly used CMOS process, image sensors with integrated "intelligence" can be designed. These sensors are very useful in many scientific, commercial and consumer applications. Current state-of-the-art CMOS imagers allow integration of all functions required for timing, exposure control, color processing, image enhancement, image compression and ADC on the same die. In addition, CMOS imagers offer significant advantages and rival traditional charge coupled devices (CCDs) in terms of low power, low voltage and monolithic integration. This lecture presents different types of CMOS pixels and introduces the system-on-a-chip approach, showing examples of two "smart" APS imagers. The camera-on-a-chip approach is introduced, focusing on the advantages of CMOS sensors on CCDs. Different types of image sensors are described and their modes of operation briefly explained. Two examples of CMOS imagers are presented, a smart vision system-on-a-chip and a smart tracking sensor. The former is based on a photodiode APS with linear output over a wide dynamic range, made possible by random access to each pixel in the array and by the insertion of additional circuitry into the pixels. The latter is a smart tracking sensor employing analog non-linear winner-take-all (WTA) selection.

Key words: CMOS image sensor, active pixel sensor (APS), charge-coupled devices (CCD), passive pixel (PS), system-on-a-chip, smart sensor, dynamic range (DR), winner-take-all (WTA) circuit.

1.1 Introduction

Driven by the demands of multimedia applications, image sensors have become a major category of high-volume semiconductor production. The introduction of imaging devices is imminent in consumer applications such as cell phones, automobiles, computer-based video, smart toys and both still and video digital cameras.

In addition to image capture, the electronics in a digital camera must handle analog-to-digital (ADC) conversion as well as a significant amount of digital processing for color imaging, image enhancement, compression control and interfacing. These functions are usually implemented with many chips fabricated in different process technologies.

The continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays a viable alternative to the popular charge-coupled devices (CCD) sensor technology. New technologies provide the potential for integrating all imaging and processing functions onto a single chip, greatly reducing the cost, power consumption and size of the camera [1–3]. Standard CMOS mixed-signal technology allows the manufacture of monolithically integrated imaging devices: all the functions for timing, exposure control and ADC can be implemented on one piece of silicon, enabling the production of the so-called "camera-on-a-chip" [4]. *Figure 1-1* is a diagram of a typical digital camera system, showing the difference between the building blocks of commonly used CCD cameras and the CMOS camera-on-a-chip. The traditional imaging pipeline functions — such as color processing, image enhancement and image compression — can also be integrated into the camera. This enables quick processing and exchanging of images. The unique features of CMOS digital cameras allow many new applications, including network teleconferencing, videophones, guidance and navigation, automotive imaging systems, and robotic and machine vision.

Most digital cameras currently use CCDs to implement the image sensor. State-of-the-art CCD imagers are based on a mature technology and present excellent performance and image quality. They are still unsurpassed for high sensitivity and long exposure time, thanks to extremely low noise, high quantum efficiency and very high fill factors. Unfortunately, CCDs need specialized clock drivers that must provide clocking signals with relatively large amplitudes (up to 10 V) and well-defined shapes. Multiple supply and bias voltages at non-standard values (up to 15 V) are often necessary, resulting in very complex systems.

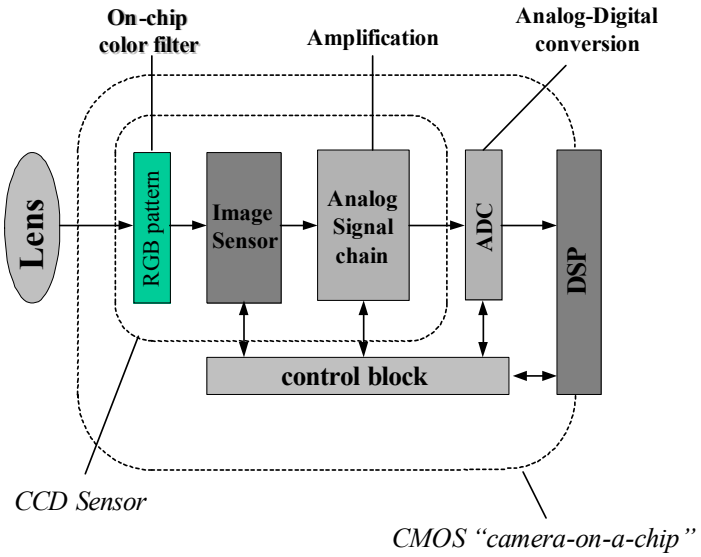


Figure 1-1. Block diagram of a typical digital camera system.

Figure 1-2 is a block diagram of a widely used interline transfer CCD image sensor. In such sensors, incident photons are converted to charge, which is accumulated by the photodetectors during exposure time. In the subsequent readout time, the accumulated charge is sequentially transferred into the vertical and horizontal CCDs and then shifted to the chip-level output amplifier. However, the sequential readout of pixel charge limits the readout speed. Furthermore, CCDs are high-capacitance devices and during readout, all the capacitors are switched at the same time with high voltages; as a result, CCD image sensors usually consume a great deal of power. CCDs also cannot easily be integrated with CMOS circuits due to additional fabrication complexity and increased cost. Because it is very difficult to integrate all camera functions onto a single CCD chip, multiple chips must be used. A regular digital camera based on CCD image sensors is therefore burdened with high power consumption, large size and a relatively complex design; consequently, it is not well suited for portable imaging applications.

Unlike CCD image sensors, CMOS imagers use digital memory style readout, using row decoders and column amplifiers. This readout overcomes many of the problems found with CCD image sensors: readout can be very fast, it can consume very little power, and random access of pixel values is possible so that selective readout of windows of interest is allowed. *Figure 1-3* shows the block diagram of a typical CMOS image sensor.

The power consumption of the overall system can be reduced because many of the supporting external electronic components required by a CCD sensor can be fabricated directly inside a CMOS sensor. Low power consumption helps to reduce the temperature (or the temperature gradient) of both the sensor and the camera head, leading to improved performance.

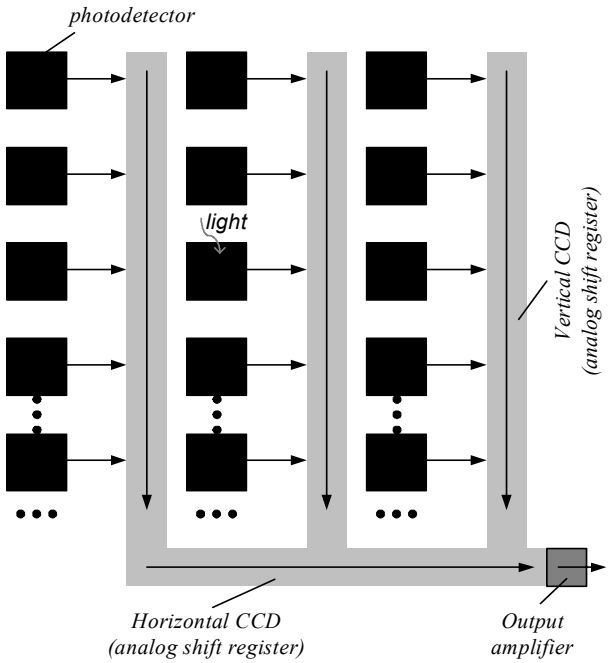


Figure 1-2. Block diagram of a typical interline transfer CCD image sensor.

An additional advantage of CMOS imagers is that analog signal processing can be integrated onto the same substrate; this has already been demonstrated by some video camera-on-a-chip systems. Analog signal processing can include widening the dynamic range of the sensor, real-time object tracking, edge detection, motion detection and image compression. These functions are usually performed by nonlinear analog circuits and can be implemented inside the pixels and in the periphery of the array. Offloading signal processing functions makes more memory and DSP processing time available for higher-level tasks, such as image segmentation or tasks unrelated to imaging.

This lecture presents a variety of implementations of CMOS image sensors, focusing on two examples of system-on-a-chip design: an image sensor with

wide dynamic range (DR) [5] and a tracking CMOS imager employing analog winner-take-all (WTA) selection [6].

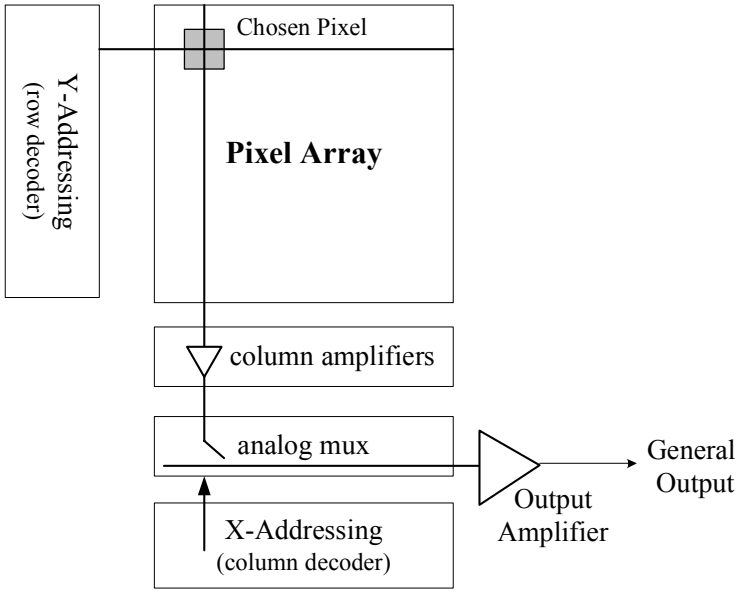


Figure 1-3. Block diagram of a typical CMOS image sensor.

1.2 CMOS image sensors

CMOS pixels can be divided into two main groups, passive pixel sensors (PPS) and active pixel sensors (APS).

Each individual pixel of a PPS array has only a photosensing element (usually a photodiode) and a switching MOSFET. The signal is detected either by an output amplifier implemented in each column or by a single output for the entire imaging device. These conventional MOS-array sensors operate like an analog DRAM, offering the advantage of random access to the individual pixels. They suffer from relatively poor noise performance and reduced sensitivity compared to state-of-the-art CCD sensors.

APS arrays are novel image sensors that have amplifiers implemented in every pixel; this significantly improves the noise parameter.

1.2.1 Passive Pixel Sensors

The PPS consists of a photodiode and just one transistor (labeled *TX* in *Figure 1-4*). *TX* is used as a charge gate, switching the contents of the pixel to the charge integration amplifier (CIA). These passive pixel CMOS sensors operate like analog DRAMs, as shown in *Figure 1-5*.

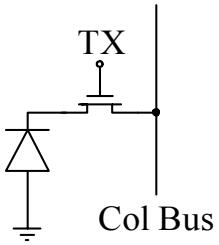


Figure 1-4. Passive pixel sensor structure.

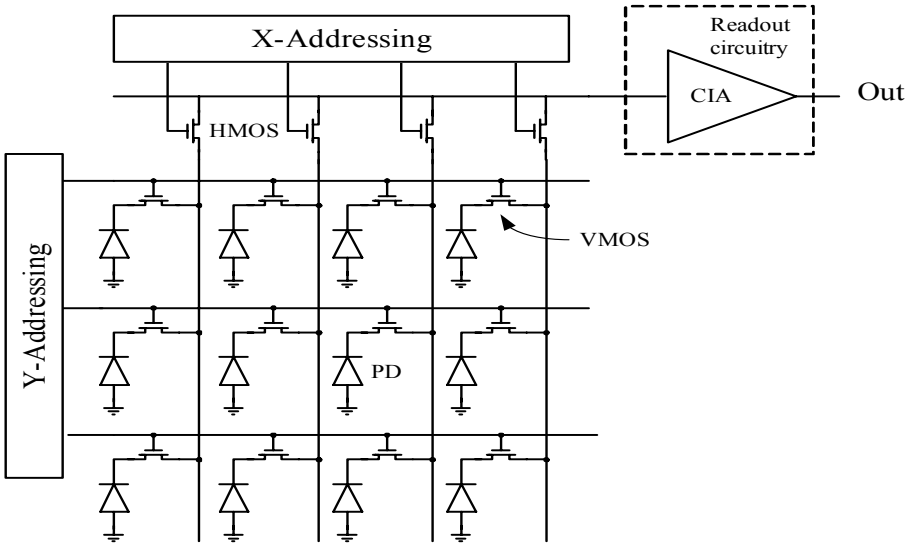


Figure 1-5. Basic PPS architecture.

More modern PPS implementations use a CIA for each column in the array, as shown in *Figure 1-6*. The CIA readout circuit is located at the bottom of each column bus (to keep the voltage on that bus constant) and uses just one addressing transistor. The voltage V_{ref} is used to reset the photo-diode

to reverse bias. Following the reset, this switch is opened, for a period of integration time (T_{int}). During this period, the photodiode discharges at a rate approximately proportional to the amount of incident illumination. When the MOS switch is closed again to reset the photodiode once more, a current flows via the resistance and capacitance of the column bus due to the difference between V_{ref} and the voltage on the diode (V_{diode}). The total charge that flows to reset the pixel is equal to that discharged during the integration period. This charge is integrated on the capacitor C_{int} and output as a voltage. When the final bus and diode voltages return to V_{ref} via the charge amplifier, the address MOS switch is turned off, the voltage across C_{int} is removed by the *Reset* transistor, and the integration process starts again.

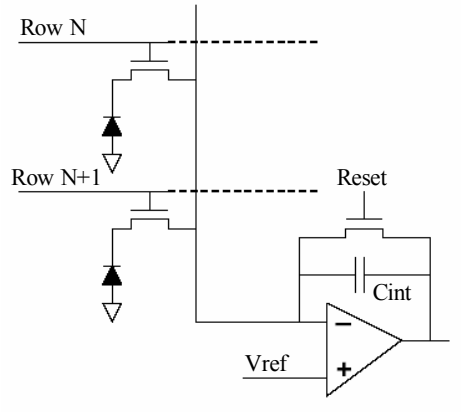


Figure 1-6. PPS implementation with a separate CIA for each column in the array (after [12]).

The passive pixel structure has major problems due to its large capacitive loads. Since the large bus is directly connected to each pixel during readout, the *RC* time constant is very high and the readout is slow. In addition, passive pixel readout noise is typically high — on the order of 250 electrons rms compared to less than 10 electrons rms for commercial CCDs. Because of these factors, PPS does not scale well to larger array sizes or faster pixel readout rates. Furthermore, differences between the individual amplifiers at the bottoms of the different columns will cause fixed pattern noise (FPN). FPN is time-independent and arises from component mismatch due to variations in lithography, doping and other manufacturing processes.

PPS also offers advantages. For a given pixel size, it has the highest design fill factor (the ratio of the light sensitive area of a pixel to its total area), since each pixel has only one transistor. In addition, its quantum efficiency (QE) —

the ratio between the number of generated electrons and the number of impinging photons — can be quite high due to this large fill factor.

1.2.2 Active Pixel Sensors

The passive pixel sensor was introduced by Weckler in 1967 [7]. The problems of PPS were recognized, and consequently a sensor with an active amplifier (a source follower transistor) within each pixel was proposed [8]. The current term for this technology, active pixel sensor, was first introduced by Fossum in 1992 [1]. *Figure 1-7* shows the general architecture of an APS array and the principal pixel structure. A detailed description of the readout procedure will be presented later in this lecture.

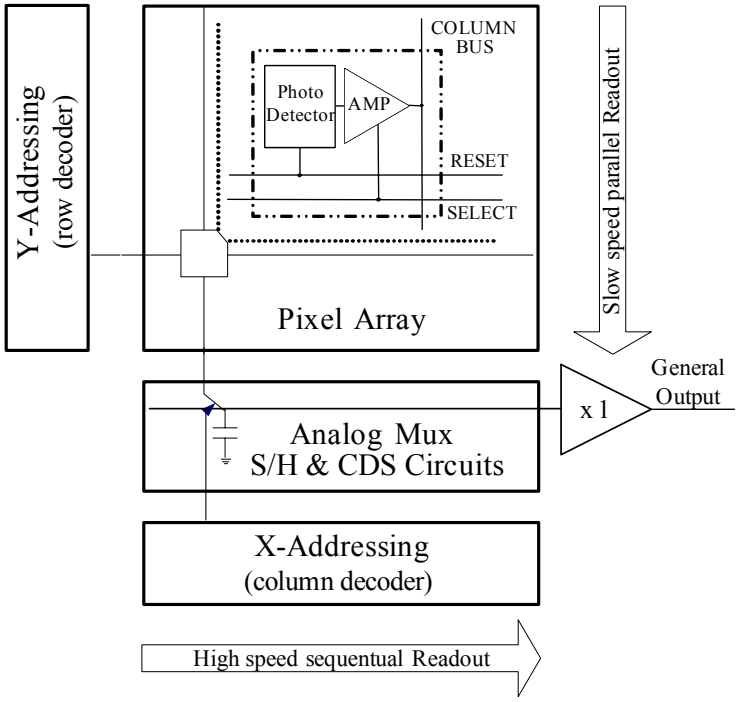


Figure 1-7. General architecture of an APS array.

Active pixels typically have a fill factor of only 50–70%, which reduces the photon-generated signal. However, the reduced capacitance in each pixel leads to lower read noise for the array, which increases both the dynamic range and the signal-to-noise ratio (SNR).

The pixels used in these sensors can be divided into three types: photodiodes, photogates and pinned photodiodes. The most popular is currently the photodiode.

1.2.3 Photodiode APS

The photodiode APS was described by Noble in 1968 [8] and has been under investigation by Andoh since the late 1980s [9]. A novel technique for random access and electronic shuttering with this type of pixel was proposed by Yadid-Pecht in the early 1990s [12].

The basic photodiode APS employs a photodiode and a readout circuit of three transistors: a photodiode reset transistor (*Reset*), a row select transistor (*RS*) and a source-follower transistor (*SF*). The scheme of this pixel is shown in *Figure 1-8*.

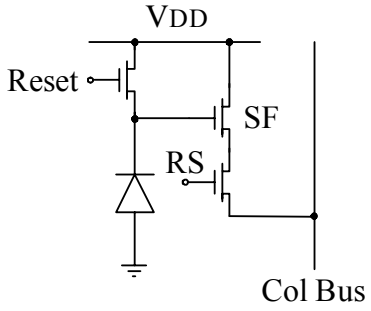


Figure 1-8. Basic photodiode APS pixel.

The charge-to-voltage conversion occurs at the sense node capacitance, which comprises the photodiode capacitance and all other parasitic capacitances connected to that node. In this case, these are the source capacitance of the *Reset* transistor and the gate capacitance of the *SF* transistor. The *SF* transistor acts as a buffer amplifier to isolate the sensing node; the load of this buffer (the active-current-source load) is located on each column rather than on each pixel to keep the fill factor high and to reduce pixel-to-pixel variations. The *Reset* transistor controls an integration time and is usually implemented with an NMOS transistor. Since no additional well is required for NMOS implementation, this allows a higher fill factor. However, an NMOS transistor with V_{DD} on both gate and drain can only reach a source voltage (at the photodiode node) of $V_{DD} - V_T$, thereby decreasing the dynamic

range of the pixel. An example of a mask layout for this pixel architecture is shown in *Figure 1-9*.

Photodiode APS operation and readout are described here with reference to both *Figure 1-7* and *Figure 1-8*. Generally, pixel operation can be divided into two main stages, reset and phototransduction.

(a) The reset stage. During this stage, the photodiode capacitance is charged to a reset voltage by turning on the *Reset* transistor. This reset voltage is read out to one of sample-and-hold (S/H) in a correlated double sampling (CDS) circuit. The CDS circuit, usually located at the bottom of each column, subtracts the signal pixel value from the reset value. Its main purpose is to eliminate fixed pattern noise caused by random variations in the threshold voltage of the reset and pixel amplifier transistors, variations in the photodetector geometry and variations in the dark current. In addition, it should eliminate the 1/*f* noise in the circuit.

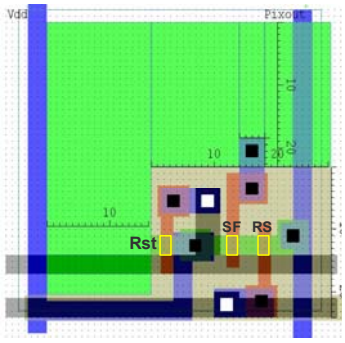


Figure 1-9. An example of a pixel layout with an L-shaped active area (in green), which is the most common pixel design.

(b) The phototransduction stage. During this stage, the photodiode capacitor is discharged through a constant integration time at a rate approximately proportional to the incident illumination. Therefore, a bright pixel produces a low analog signal voltage and a background pixel gives a high signal voltage. This voltage is read out to the second S/H of the CDS by enabling the row select transistor of the pixel. The CDS outputs the difference between the reset voltage level and the photovoltage level.

Because the readout of all pixels cannot be performed in parallel, a rolling readout technique is applied. All the pixels in each row are reset and read out

in parallel, but the different rows are processed sequentially. *Figure 1-10* shows the time dependence of the rolling readout principle. A given row is accessed only once during the frame time (T_{frame}). The actual pixel operation sequence is in three steps: the accumulated signal value of the previous frame is read out, the pixel is reset, and the reset value is read out to the CDS. Thus, the CDS circuit actually subtracts the signal pixel value from the reset value of the next frame. Because CDS is not truly correlated without frame memory, the read noise is limited by the reset noise on the photodiode. After the signals and resets of all pixels in the row are read out to S/H, the outputs of all CDS circuits are sequentially read out using X-addressing circuitry, as shown in *Figure 1-7*.

The output photodiode signal is supposedly independent of detector size, because the lower pixel capacitance of smaller detectors causes an increase in conversion gain that compensates for the decrease in detector size. However, peripheral capacitances from the perimeters of the detector increase the total capacitance of the sensing node and thus decrease the conversion gain. As the pixel size scales down, photosensitivity decreases and the reset noise scales as $C^{1/2}$, where C is the photodiode capacitance. These tradeoffs must be considered when designing pixel fill factor, DR, SNR and conversion gain.

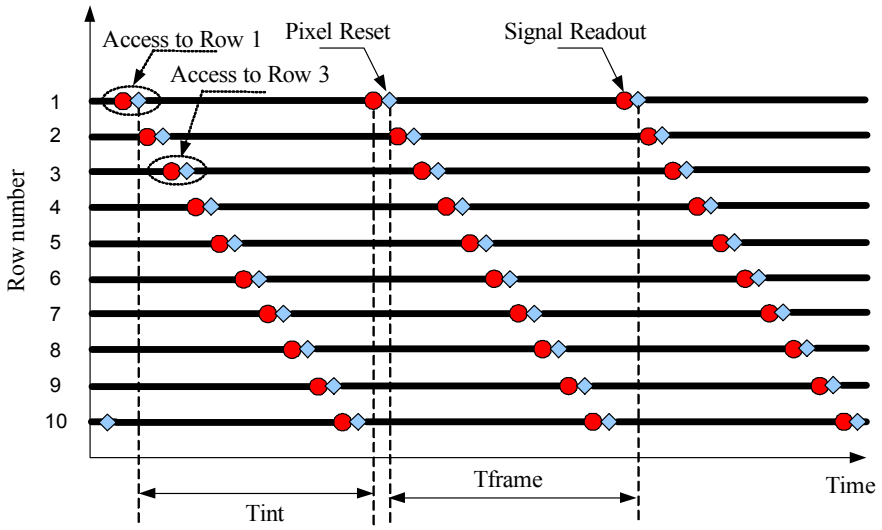


Figure 1-10. Rolling readout principle of the photodiode APS.

1.2.4 Photogate APS

Figure 1-11 shows the common photogate pixel architecture [10]. The basic concept for the photogate pixel arose from CCD technology. While photon-generated charge is integrated under a photogate with a high potential well, the output floating node is reset and the corresponding voltage is read out to the S/H of the CDS. When the integration is completed, the charge is transferred to the output floating node by pulsing the signal on the photogate. Then the corresponding voltage from the integrated charge is read by the source follower to the second S/H of the CDS. The CDS outputs the difference between the reset voltage level and the photo-voltage level.

As mentioned above, the CDS can suppress reset noise, $1/f$ noise and FPN due to V_T and lithographic variations in the array. The reduction of noise level increases the total dynamic range and the SNR. The primary noise source for the photogate APS is photon shot noise, which cannot be suppressed by any means.

The photogate has a pixel pitch typically equal to 20 times the minimum size of the technology, since there are five transistors in each pixel. Due to the overlaying polysilicon, however, there is a reduction in QE, particularly in the blue region of the spectrum.

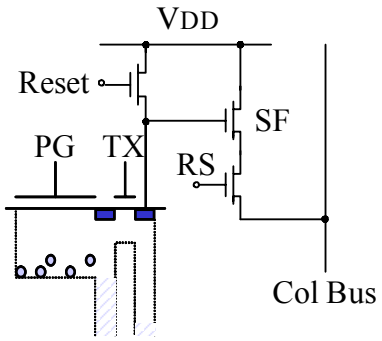


Figure 1-11. Basic photogate pixel architecture.

The photogate pixel architecture is shown as a mask layout in *Figure 1-12*.

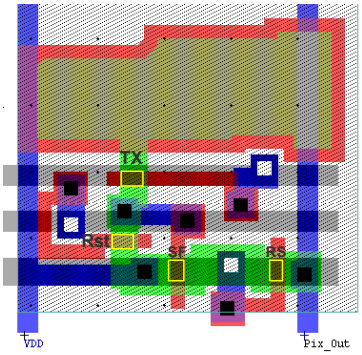


Figure 1-12. Example layout of a photogate pixel design.

1.2.5 Pinned photodiode APS

The pinned photodiode pixel consists of a pinned diode (p^+-n-p), where the photon collection area is dragged away from the surface in order to reduce surface defect noise (such as that due to dark current) [12]. Photon-generated charge is integrated under a pinned diode and transferred to the output floating diffusion for the readout. As in the photogate APS, the sense node and integration node are separated to minimize noise. However, the primary difference is that the potential well for charge collection in a pinned diode is generated by a buried intrinsic layer (or an n-type layer) instead of a pulsed gate voltage as in the photogate. Each pinned diode pixel has four transistors and five control lines, resulting in a fill factor higher than in the photogate pixel, but lower than in the photodiode pixel. However, the small photon collection area of the pinned diode results in a very small full well for photon-generated charge collection and lower QE compared to the photodiode pixel. *Figure 1-13* shows a basic pinned photodiode pixel structure.

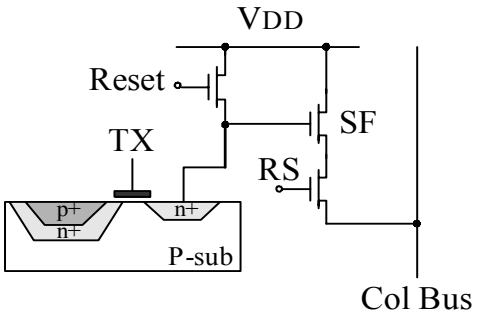


Figure 1-13. Basic pinned photodiode pixel architecture.

1.2.6 Logarithmic Photodiode APS

Another type of APS is a logarithmic photodiode sensor [11]. This three-transistor pixel enables logarithmic encoding of the photocurrent, thus increasing the dynamic range of the sensor; i.e., the same range of sensor output voltage is suitable for a wider range of illumination. The implementation of the basic logarithmic photodiode pixel is described in *Figure 1-14*.

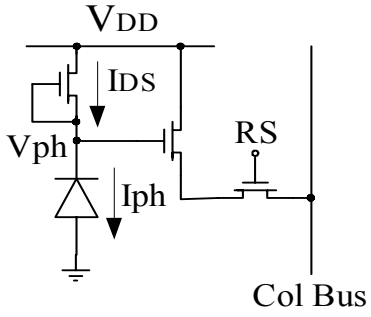


Figure 1-14. Basic logarithmic photodiode pixel architecture.

This pixel does not require reset and operates continuously. The voltage on the photodiode (V_{PH}) is approximately equal to V_{DD}, causing the load transistor to operate in the subthreshold region ($V_{DD} = V_{PH} + \Delta V_{PH}$). The photocurrent ($I_{PH}$) is equal to the subthreshold current (I_{DS}). The voltage on

the photodiode decreases logarithmically with linear increases in illumination (and thus photocurrent) following the equation

$$V_{\mathrm{PH}} = V_{\mathrm{DD}} - \Delta V_{\mathrm{PH}} = V_{\mathrm{DD}} - \frac{KT}{q} \cdot \ln\left(\frac{I_{\mathrm{PH}}}{I_0}\right) \tag{1.1}$$

where KT/q is 0.026 V at $T = 300$ K and I_0 represents all constant terms. While the logarithmic APS has the above-mentioned advantages, it suffers from serious drawbacks such as significant temperature dependence of the output, low swing of the output (especially for relatively low illumination levels) and high FPN. Accordingly, the logarithmic APS is not commonly used.

1.2.7 Snapshot pixels

Most CMOS imagers feature the rolling shutter readout method (also known as the rolling readout method) shown in *Figure 1-10*. In the rolling shutter approach, the start and end of the light collection for each row is slightly delayed from the previous row; this leads to image deformity when there is relative motion between the imager and the scene. The ideal solution for imaging objects moving at high speed is the snapshot imager, which employs the electronic global shutter method [12]. This technique uses a memory element inside each pixel and provides capabilities similar to a mechanical shutter: it allows simultaneous integration of the entire pixel array and then stops the exposure while the image data is read out. The principal scheme of snapshot photodiode APS was introduced by Yadid-Pecht in 1991, and is shown in *Figure 1-15*.

The snapshot pixel includes a sample-and-hold (S/H) switch with analog storage, which consists of all parasitic capacitances in the amplifier input. The in-pixel amplification is performed by a source follower amplifier, identical to that in a rolling shutter pixel. The full transistor scheme of a commonly used global shutter pixel is shown in *Figure 1-16*.

In contrast to the rolling shutter technique, a sensor with global shutter architecture exposes all its pixels at the same time. After the integration time T_{int}, the signal charge is stored in an in-pixel sample-and-hold capacitance until readout. One of the problems that should be addressed in the snapshot pixels is the shutter efficiency. The light exposure of the S/H stage, shutter leakage and the limited storage capacitance lead to signal lost. *Figure 1-16* shows a pixel that employs an NMOS transistor as a shutter. This

implementation allows a small pixel area, but it has a low shutter efficiency. Shutter efficiency can be increased using a PMOS transistor as a shutter, if it is well separated from the photodiode. Unfortunately, a PMOS shutter decreases the fill factor and, due to increased parasitic capacitances, also decreases the conversion gain.

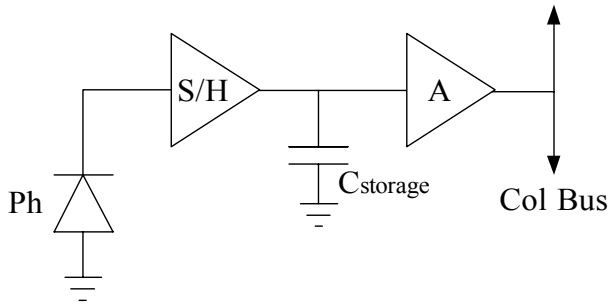


Figure 1-15. Architecture of a snapshot photodiode APS (after [12]).

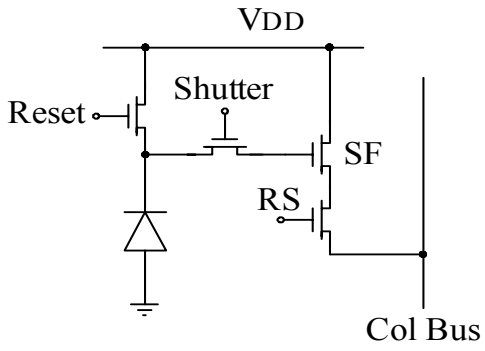


Figure 1-16. Transistor scheme of a commonly used snapshot pixel.

1.3 APS system-on-a-chip approach

CMOS image sensors allow implementations of complex sensing systems on a single silicon die. For example, almost all CMOS imagers employ analog to digital conversion on the same die. There are three general approaches to implementing ADC with active pixel sensors:

1. Chip-level ADC, where a single ADC circuit serves the whole APS array. This method requires a very high-speed ADC, especially if a very large array is used.
2. Column-level ADC, where an array of ADCs is placed at the bottom of the APS array and each ADC is dedicated to one or more columns of the APS array. All these ADCs are operated in parallel, so a low-to-medium-speed ADC design can be used, depending on the APS array size. The disadvantages of this approach are the necessity of fitting each ADC within the pixel pitch (i.e., the column width) and the possible problems of mismatch among the converters on different columns.
3. Pixel-level ADC, where every pixel has its own converter. This approach allows parallel operation of all ADCs in the APS array, so a very low speed ADC is suitable. Using one ADC per pixel has additional advantages, such as higher SNR, lower power and simpler design.

In this section, two examples of CMOS imagers are described. The first implements a "smart vision" system-on-a-chip based on a photodiode APS with linear output over a wide dynamic range. An increase in the dynamic range of the sensors is enabled by random access to the pixel array and by the insertion of additional circuitry within each pixel. The second example is a smart tracking sensor employing analog nonlinear winner-take-all selection.

In the design of a "smart" sensing system, an important step is to decide whether computation circuitry should be inserted within the pixel or placed in the periphery of the array. When processing circuitry is put within the pixel, additional functions can be implemented, simple 2-D processing is possible, and neighboring pixels can be easily shared in neural networks. These systems are also very useful for real-time applications. On the other hand, the fill factor is drastically reduced, making these systems unsuitable for applications where high spatial resolution and very high image quality are required. In all systems presented later in this lecture, most of the processing circuitry is placed in the periphery of the array to avoid degradation of image quality.

1.3.1 Autoscaling APS with customized increase of dynamic range

This section introduces the reader to the dynamic range problem in CMOS imagers, showing possible existing solutions. Then an advanced autoscaling CMOS APS with customized linear increase of DR is explained.

1.3.1.1 Dynamic range problem and possible solutions

Scenes imaged with electronic cameras can have a wide range of illumination. Levels can range from 10^{-3} lux for night vision to 10^{5} lux for scenes illuminated with bright sunlight, and even higher levels can occur with the direct viewing of light sources such as oncoming headlights. The intrascene dynamic range capability of a sensor is measured as

$$DR = 20 \cdot \log(S/N) \tag{1.2}$$

where S is the saturation level and N is the root mean square (rms) read noise floor measured in electrons or volts. The human eye has a dynamic range of about 90 dB and camera film of about 80 dB, but typical CCDs and CMOS APS have a dynamic range of only 65–75 dB. Generally, dynamic range can be increased in two ways: the first one is noise reduction and thus expanding the dynamic range toward darker scenes. The second method is incident light saturation level expansion, thus improving the dynamic range toward brighter scenes.

Bright scenes and wide variations in intrascene illumination can arise in many situations: driving at night, photographing people in front of a window, observing an aircraft landing at night, and imaging objects for studies in meteorology or astronomy. Various solutions have been proposed in both CCD and CMOS technologies to cope with this problem [13-37]. Methods for widening the dynamic range can be grouped into five areas:

1. Companding sensors, such as logarithmic compressed-response photodetectors;
2. Multi-mode sensors, where operation modes are changed;
3. Frequency-based sensors, where the sensor output is converted to pulse frequency;
4. Sensors with external control over integration time, which can be further divided into global control (where the integration time of the whole sensor can be controlled) and local control (where different areas within the sensor can have different exposure times); and
5. Sensors with autonomous control over integration time, in which the sensor itself provides the means for different integration times.

Companding sensors. The simplest solution to increase DR is to compress the response curve using a logarithmic photodiode sensor, as described in section 1.2.6. Another type of companding sensor for widening the DR was introduced by Mead [16], where a parasitic vertical bipolar transistor with a logarithmic response was used. The logarithmic function there is again a

result of the subthreshold operation of the diode-connected MOS transistors, added in series to the bipolar transistor. The voltage output of this photoreceptor is logarithmic over four or five orders of magnitude of incoming light intensity. It has been used successfully by Mahowald and Boahen [17]. This detector operates in the subthreshold region and has a low output voltage swing. A disadvantage of these pixels is that this form of compression leads to low contrast and loss of details; adaptation, where linearity around the operation point is exploited, was proposed to alleviate this problem [18–19]. Also, the response of the logarithmic pixels with this kind of readout is light dependent. This means that for low light intensities the readout time would be very slow, depending also on the photodiode capacitance.

Multimode sensors. A multisensitivity photodetector was proposed by Ward et al. [21]. The detector is a parasitic vertical bipolar transistor between diffusion, well and substrate. By connecting a MOS transistor to the base and the emitter of the bipolar transistor in a Darlington structure, the current gain can be boosted further. Thus, both bipolar transistors can be activated at very low light intensities and inactivated at higher intensities. For moderate levels, only one bipolar transistor is activated. Two selection transistors are required within the pixel for choosing the mode. This pixel occupies a relatively large area.

Frequency-based sensors. In 1994, Yang [22] proposed a pulse photosensor that uses simple integrate-and-reset circuitry to directly convert optical energy into a pulse frequency output. The output of this photosensor can vary over 5–6 orders of magnitude and is linearly proportional to optical energy. A diagram of the circuitry is presented in *Figure 1-17*.

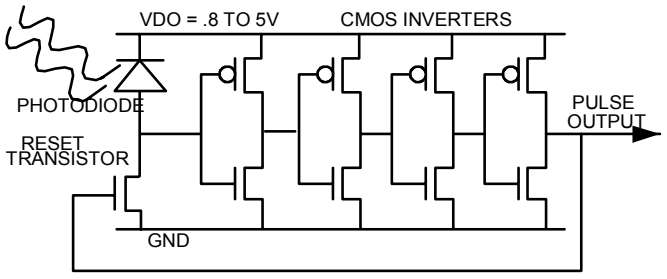


Figure 1-17. A pulse photosensor with reset circuitry (after Yang).

The pixel fill factor is much decreased with this approach, since the inverter chain resides next to the photodiode. In addition, the pulse timing

relies on the threshold voltages of the inverters. Since threshold voltage mismatches exists between different transistors, there will be a different response for each pixel. This makes this sensor worse in terms of noise, since the threshold mismatch translates to a multiplicative error (the output frequency of the pulses is affected) and not just constant FPN.

Sensors with external control over integration time. A multiple-integration-time photoreceptor has been developed at Carnegie Mellon University [23]. It has multiple integration periods, which are chosen depending upon light intensity to avoid saturation. When the charge level nears saturation, the integration is stopped at one of these integration periods and the integration time is recorded. This sensor has a very low fill factor.

Sensors with autonomous control over integration time. The automatic wide-dynamic-range sensor was proposed by Yadid-Pecht [24, 25]. This imager consisted of a two-dimensional array of sensors, with each sensor capable of being exposed for a different length of time with autonomous on-chip control. Reset enable pulses are generated at specific times during the integration period. At each reset enable point, a nondestructive readout is performed on the sensor and compared to a threshold value. A conditional reset pulse is generated if the sensor value exceeds the threshold voltage. The main drawback with this solution is the extent of the additional circuitry, which affects spatial resolution.

In the following sections, we describe an APS with an in-pixel autoexposure and a wide-dynamic-range linear output. Only a minimum additional area above the basic APS transistors is required within the pixel, and the dynamic range enhancement is achieved with minimal effects on the temporal resolution.

1.3.1.2 System architecture

The architecture of the DR approach is shown in *Figure 1-18*.

As in a traditional rolling-shutter APS, this imager is constructed of a two-dimensional pixel array, here of 64 columns and 64 rows, with random pixel access capability. Each pixel contains an optical sensor to receive light, a reset input and an electrical output representing the illumination received. The pixel used here is not a classic pixel, since it enables individual pixel reset via an additional transistor [5]. The outputs of a selected row are read through the column-parallel signal chain, and at certain points in time are also compared with an appropriate threshold in the comparison circuits. If a pixel value exceeds the threshold, a reset is given at that time to that pixel. The binary information concerning the reset (i.e., applied or not) is saved in digital storage for the later calculation of the scaling factor. The pixel value can then

be determined as a floating-point number, where the exponent comes from the scaling factor for the actual integration time and the mantissa from the regular A/D output. Therefore, the actual pixel value would be

$$Value = Man \cdot \left(T \Big/ \left(T / X^{EXP} \right) \right) = Man \cdot X^{EXP} \tag{1.3}$$

where *Value* is the actual pixel value, *Man* (mantissa) is the analog or digitized output value that has been read out at the time T, X is a constant greater than one (for example, 2), and *EXP* is the exponent value describing the scaling factor. This digital value is read out at the upper part of the chip. For each pixel, only the last readouts of a certain number of rows are kept to enable the correct output for the exponent bits.

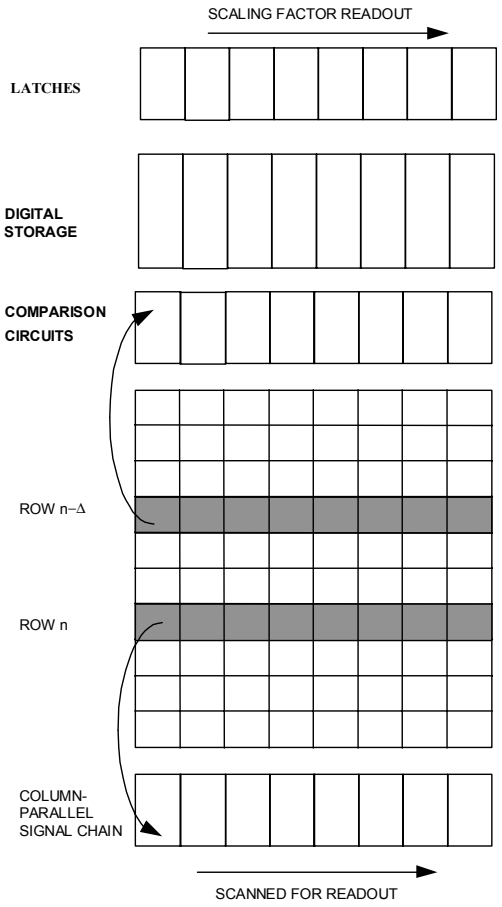


Figure 1-18. General architecture description of the autoscaling CMOS APS.

The idea of having a floating-point presentation per pixel via real-time feedback from the pixel has been proposed before by Yadid-Pecht [36]. However, the previous design required an area in the pixel that substantially affected the fill factor, so it was then proposed that the control for a group of pixels should be shared. In the currently proposed solution, however, the necessary additional hardware will be placed in the periphery; as a result, the information can be output with minimal effect on spatial or temporal resolution. The spatial resolution is slightly modified, since the desired ability to independently reset each pixel requires an additional transistor per pixel [37]. Concerning the temporal resolution - for a certain pixel we should check at different time points to get the exponential (scaling) term. Equivalently, we

could look at the pixels of different rows to get the same information. In the latter case, row n at time zero would provide the mantissa for row n (either through an on-chip or an off-chip A/D output), while the pixels in row $n - N/2$ (where N is the total number of rows that set the frame time) would provide the first exponent bit (W_1) as a result of the logic circuit decision for that row. Row $n - N/4$ would provide the second bit (W_2) for that row, row $n - N/8$ would provide the third bit, and so on. Thus, at the cost of a customized number of comparisons, the required information can be obtained automatically and the mantissa scaled accordingly.

Figure 1-19 describes this approach via a combined time-space diagram where the axes represent the row number and time, respectively. W_1, W_2, ... W_w, represent the exponent bits; i.e., W_1 represents the first point of decision $T - T/2$ (whether to reset or not for the first time), W_2 for the next point and so forth. The equivalent is shown at point $n - N/2$ in the spatial domain, which is the row that should be used for the decision concerning W_1.

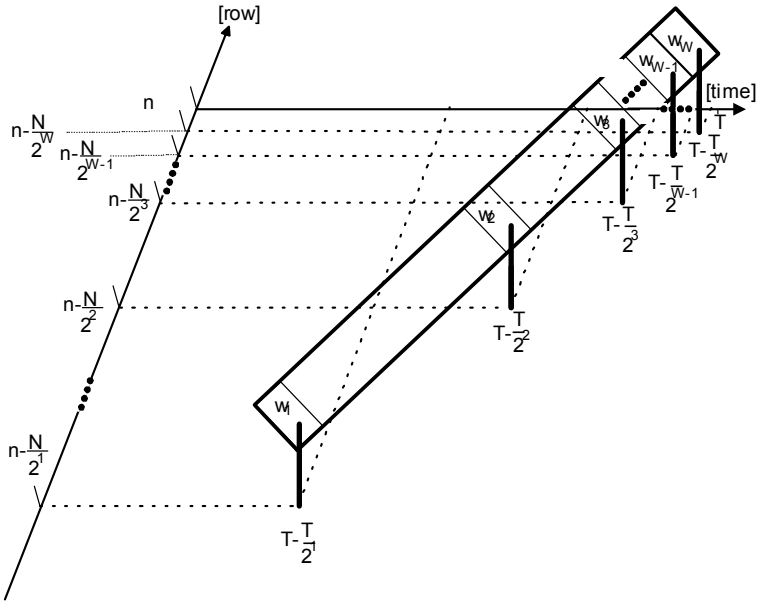


Figure 1-19. Combined time-space diagram.

For example, an imaging device consisting of a square pixel array of 64 rows and 64 columns may be assumed, and it is desired to expand the dynamic range by 3 bits due to a high illumination level. Therefore, $W = 3$ and $N = 64$ in this case. For each pixel from the selected row n, three comparisons (W_1, W_2 and W_3) are carried out at three corresponding time points ($T - T/2$, $T - T/4$, $T - T/8$). The first comparison, which is with the threshold, is carried out at row $n - 32$ (32 rows before regular readout of that pixel). This leaves an integration time of $T/2$ with a comparison result of W_1 = "1", and this pixel is reset. The second comparison is carried out at row $n - 16$ (16 rows before regular readout of that pixel), leaving an integration time of $T/4$ with a comparison result of W_2 = "1"; this pixel is also reset. The third comparison is carried out at row $n - 8$ (8 rows before regular readout of that pixel), leaving an integration time of $T/8$ with a comparison result of W_3 = "1". This pixel is reset as well. The autoscaling combination for the pixel in this example is therefore (1 1 1): this means that the pixel has been reset three times during the frame time, and the regular readout for this pixel should be scaled (multiplied) by a factor of $2^3 = 8$.

The frame time of a pixel array consisting of N rows and N columns may be calculated. Readout time for each row is composed of a copying time (T_{copy} = the time needed to copy one row into the readout buffer) and a scanning time (T_{scan} = the time needed to scan each pixel). Since there are N pixels in each row, the total time for row readout (T_{row}) is given by

$$T_{row} = T_{copy} + N \times T_{scan} \tag{1.4}$$

and the frame time (T_{frame}) is given by

$$T_{frame} = N \times T_{scan} \tag{1.5}$$

By adding W comparisons (for W different integration times) for each row, the row readout time is slightly modified and is given by

$$\begin{aligned} T'_{row} &= W \times T_{comp} + T_{row} \\ &= W \times T_{comp} + T_{copy} + N \times T_{scan} \end{aligned} \tag{1.6}$$

where T_{comp} is the time for comparison to the threshold level. Since $W << N$ then

$$W \times T_{comp} << N \times T_{scan} \tag{1.7}$$

and $T'_{\text{row}} = T_{\text{row}}$. Hence, the frame time T_{frame} is insignificantly affected by autoscaling. This enables the imager to process scenes without degradation in the frame rate.

1.3.1.3 Design and implementation

A block diagram of the proposed design is shown in *Figure 1-20*. The design makes use of a column parallel architecture to share the processing circuits among the pixels in a column. The pixel array, the memory array and the processing elements are separated in this architecture. Each pixel contains an additional transistor (in series with the row reset transistor) that is activated by a vertical column reset signal; this allows the independent reset of the pixel. Integration time can be adjusted for each pixel with this reset, and nondestructive readout of the pixel can be performed at any time during the integration period by activating the row select transistor and reading the voltage on the column bus.

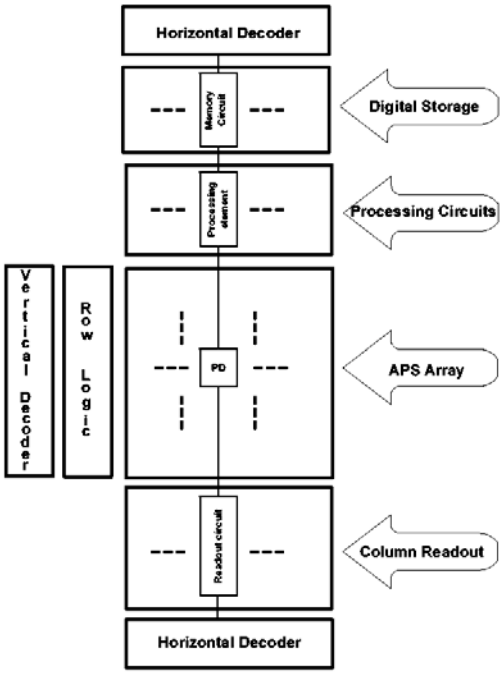


Figure 1-20. Block diagram of the proposed design.

The processing element contains the saturation detection circuit, which is shared by all pixels in a column. Because of the column parallel architecture, the pixel array contains a minimum amount of additional circuitry and sacrifices little in fill factor. The memory array contains the SRAMs and latches. Two horizontal decoders — one each for the pixel array and the memory array — work in parallel and are used to retrieve the mantissa and exponent, respectively. The vertical decoder is used to select the rows in order.

The electrical scheme for a single column is presented in *Figure 1-21*.

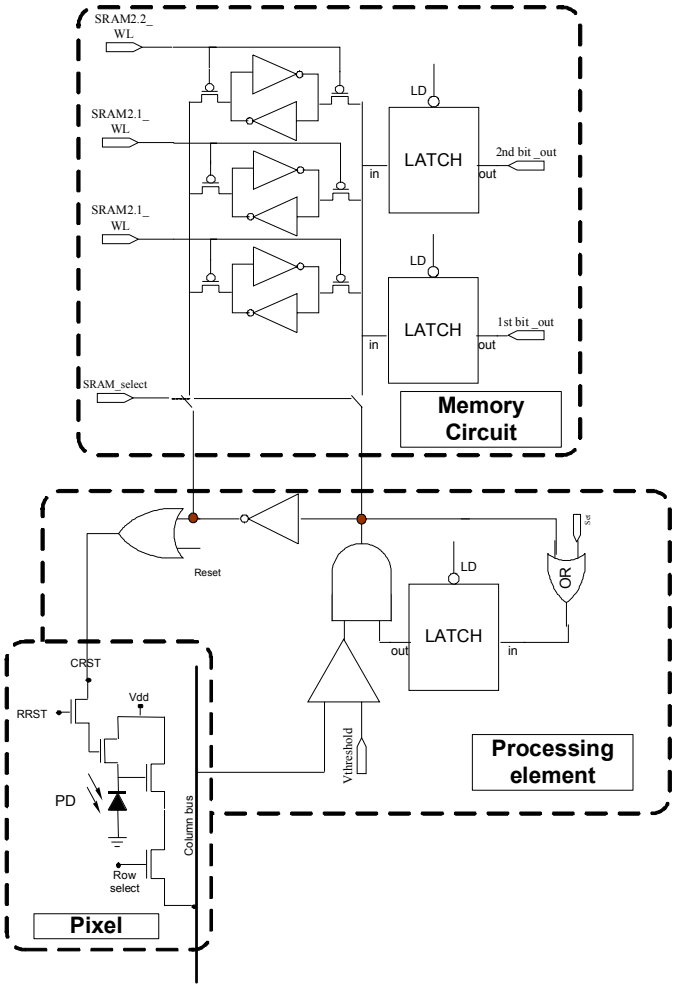


Figure 1-21. Electrical description of one column of an autoscaling CMOS APS.

In this circuit, the pixel output signal is evaluated at the comparator, where it is compared with an appropriate threshold. If its signal exceeds a predetermined threshold, the pixel is detected as saturated. Using this information and the binary information concerning the pixel (stored in the memory during different parts of the integration), a decision whether to reset the pixel is made. If the decision is positive, the column reset (*CRST*) and row reset (*RRST*) lines must both be precharged at a logical high voltage to activate the reset transistor; the photodiode then restarts integration. If the decision is negative, the reset is not active and the pixel continues to integrate.

The binary information (whether the reset was applied or not) is saved in the SRAM memory storage and output to the latches in due time. After the row is read through the regular output chain, this additional information is retrieved from the memory through the latches.

1.3.1.4 Experimental results

A 64 × 64 pixel chip was successfully fabricated using the HP 0.5 μm n-well process. The chip photograph is shown in *Figure 1-22*. The sensor was quantitatively tested for relative responsivity, conversion gain, saturation level, noise, dynamic range, dark current and fixed pattern noise. The results are presented in *Table 1-1*.

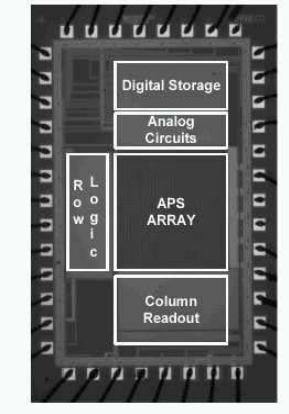


Figure 1-22: Photograph of the fabricated autoscaling CMOS APS test chip.

The conversion gain was in general agreement with the design estimate of photodiode capacitance. The saturation level was approximately 1.33 V; fixed pattern noise (FPN) was measured to be approximately 0.15% saturation; dark current was measured to be on the order of 30–35 mV/sec, output referred, or 0.61 pA/cm^2; and the inherent dynamic range was 71.4 dB, or 11 bits. The extended dynamic range provided two additional bits to the inherent dynamic range. No smear or blooming was observed due to the lateral overflow drain inherent in the APS design. The chip was also functionally tested.

Table -1. Attributes of the autoscaling CMOS APS test chip.

Chip format	64 × 64 pixels
Chip technology	HP 0.5 μm

Chip format	64 × 64 pixels
Chip size	1.878 mm × 2.9073 mm
Pixel size	14.4 μm × 14.4 μm
Pixel type	Photodiode
Pixel fill factor	37%
Conversion gain	12 μV/e^-
Fixed pattern noise (FPN)	0.15%
Dark current (room temp)	35 mV/sec (0.61 pA/cm^2)
Power	3.71 mW (5 Mhz)
Inherent dynamic range	71.4 dB (~11 bit)
Extended dynamic range	2 additional bits
Saturation level	1.33 V
Quantum efficiency (QE)	20%

Figure 1-23 shows a comparison between an image captured by a traditional CMOS APS and by the autoexposure system presented here. In the *Figure 1-23(a)*, a scene is imaged with a strong light on the object; hence, some of the pixels are saturated. At the bottom of *Figure 1-23(b)*, the capability of the autoexposure sensor for imaging the details of the saturated area in real time may be observed. Since the display device is limited to eight bits, only the most relevant eight-bit part (i.e., the mantissa) of the thirteen-bit range of each pixel is displayed here. The exponent value, which is different for different areas, is not displayed. This concept in its present form suits rolling-shutter sensors, and a first prototype following this concept has been demonstrated here.

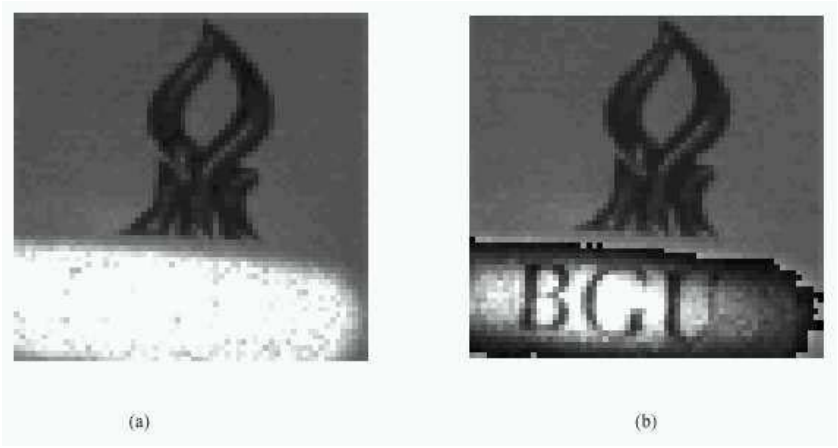


Figure 1-23. (a) Scene observed with a traditional CMOS APS sensor.(b) Scene observed with the in-pixel autoexposure CMOS APS sensor.

1.3.2 CMOS smart tracking sensor employing WTA selection

This section presents an example of a smart APS sensor suitable for tracking purposes. The system employs an analog winner-take-all circuit to find and track the brightest object in the field of view (FOV). This system-on-a-chip employs adaptive spatial filtering of the processed image, with elimination of bad pixels and with reduction of false alarm when the object is missing. The circuit has a unique adaptive spatial filtering ability that allows the removal of the background from the image, and this occurs one stage before the image is transferred to the WTA detection circuit. A test chip of 64×64 array has been implemented in 0.5 μm CMOS technology. It has a 49% fill factor, it is operated by 3.3 V supply, and it dissipates 36 mW at video rate. The system architecture and operation are described, together with measurements from a prototype chip.

1.3.2.1 Motivation

Many scientific, commercial and consumer applications require spatial acquisition and tracking of the brightest object of interest. A winner-take-all function has an important role in these kinds of systems: it selects and identifies the highest input (which corresponds to the brightest pixel of the sensor) and inhibits the rest. The result is a high digital value assigned to the winner pixel and a low one assigned to the others. CMOS implementations of WTA networks are an important class of circuits widely used in neural networks and pattern-recognition systems [42, 44]. Many WTA circuit implementations have been proposed in the literature [40–52]. A current-mode MOS implementation of the WTA function was first introduced by Lazzaro [40]. This very compact circuit optimizes power consumption and silicon area usage. It is asynchronous, responds in real time and processes all input currents in parallel.

Most of the existing WTA circuits can be integrated with APS sensors. Usually, when WTA circuits are used in two-dimensional tracking and visual attention systems, the image processing circuitry is included in the pixel; however, there are penalties in fill factor or pixel size and resolution. Here we show an implementation of a 2-D tracking system using 1-D WTA circuits. All image processing is performed in periphery of the array without influencing imager quality.

As mentioned above, the regular WTA circuit chooses a winner from a group of input signals. When an APS with WTA selection system is used for object selection, a number of problems can occur. If the object of interest disappears from the processed image, the WTA will compare input voltages

that represent intensity levels in the image background; hence, the circuit will output the coordinates of some background pixel instead of the missing object of interest and cause a false alarm. Background filtering and false alarm reduction is therefore necessary. Another problem that can disrupt proper operation of the system is a bad pixel. Since the bad pixel has a high value, it can be selected as the winner regardless of other pixel values.

The simplest technique for background filtering is signal comparison against a globally set threshold, above which pixels qualify as object pixels. The disadvantage of this kind of filtering is that it is necessary to choose the value of this threshold in advance; in the case where the background is overly bright (i.e., above the chosen threshold), the circuit will not be able to cope with the task. The problem is most severe if the object of interest disappears from the processed image and the background is bright.

The system described here is a 64×64 element APS array with two-dimensional WTA selection. A spatial adaptive filtering circuit allows adaptive background filtering and false alarm reduction if the object is missing from the scene.

1.3.2.2 System architecture

Figure 1-24 shows the block diagram of the system. There is no penalty in spatial resolution using the proposed architecture, since the processing is done at the periphery of the array.

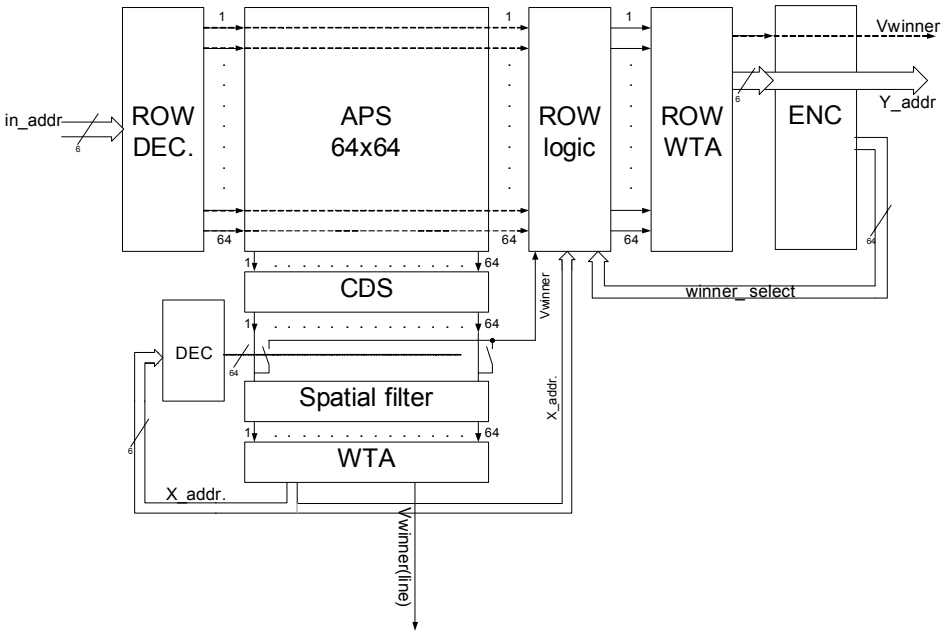


Figure 1-24. Block diagram of the proposed CMOS smart tracking sensor system.

The process of phototransduction in the APS is done row-by-row in two phases: reset (where a photodiode capacitor is charged to a high reset voltage) and phototransduction (where the capacitor is discharged after a constant integration time). A commonly used CDS circuit is implemented on the chip to subtract the signal pixel value from the reset one; the output is high for a bright pixel and low for a dark one. The subsequent stage is adaptive background filtering of all pixels for which the CDS values are less than a threshold value. This threshold corresponds to the average of the outputs from all row sensors, with the addition of a small variable epsilon value. Only the signals that pass the filter are transmitted to the WTA selection circuit. When there is no detectable object (i.e., only background signals exist), no signals pass this filter, and so the "no object" output becomes high and false alarm reduction is achieved. A detailed description of this filtering technique is presented in section 1.3.2.3.

The next stage is the winner-take-all selection, which is done with a simple voltage-mode WTA after Donckers et al. [48]. The main factor for choosing this WTA circuit is its simplicity; generally any kind of voltage- or current-mode WTA can be integrated with this system [53]. The winner selection is

done row-by-row. The winner of each row is found, its value is stored into an analog memory (a capacitor), and its address is deposited in the digital storage. If there is more than one input with the same high value, the WTA chooses the leftmost one using a simple logic. The result is a column of N analog pixel values of row winners with their column addresses. From all the row winners, a global winner is selected using an identical WTA circuit. The 1-D winner selection array was designed to consist of eight identical blocks of eight-input WTA cells to achieve better resolution and reduce matching problems. The row winner value is stored in the analog memory that corresponds to the actual row and its column address is stored in the corresponding digital memory; these analog and digital memories are in the *ROW logic* block displayed in *Figure 1-24*. In the case of "no object" in a row, the value transmitted to the memory is zero. Following a full frame scan, the WTA function is activated on all 64 row winners (in the *ROW WTA* block in *Figure 1-24*) and the location of the global frame winner is found. Its analog value and its address are then read out of the memory by an encoder (the *ENC* block in *Figure 1-24*).

This architecture allows the enlargement of the proposed system to any size of $N \times N$ pixel array without affecting the system properties.

1.3.2.3 Descriptions of the circuits

1.3.2.3.1 The adaptive spatial filter

The principal scheme of the adaptive 1-D filter circuit used in the CMOS smart tracking sensor system is shown in *Figure 1-25*. The inputs to the filter correspond to the CDS values, and the outputs are the control signals. As mentioned earlier, this circuit filters all pixels for which the CDS values are less than a threshold value. This threshold corresponds to the average of the outputs from all the row sensors, with the addition of a small variable epsilon value. The *Control* output of the filter is high for an object pixel and low for a pixel that is imaging the background. The advantage of this filtering is that this epsilon value is adaptive and not constant for different input vectors. The value of epsilon depends inversely on the average current value: it increases when the average current decreases and decreases when current increases. This results in a small epsilon value for a high background and a high epsilon for a low background. The filtering process is thus more sensitive when a high background is present and the input voltage of the object is very similar to that of the background. The epsilon value can be controlled manually by setting suitable V- and V+ voltage values (see *Figure 1-25*).

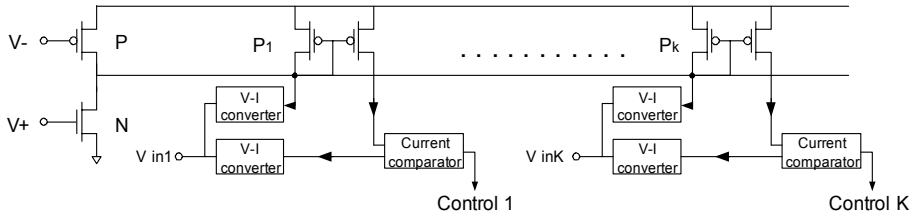


Figure 1-25. Principal scheme of the spatial filter circuit in the CMOS smart tracking sensor.

If $V+$ is zero and $V-$ is V_{DD}, then the epsilon value is zero and all $I_{average} + \varepsilon$ currents of the circuit are equal to the average current of the n inputs in an n-sized array. The non-zero epsilon value can be added to this average by increasing the $V+$ value. The epsilon value can also be subtracted from the average by decreasing the $V+$ value. A positive epsilon value is usually of interest here, so $V-$ is V_{DD} in this case. Note that the voltages to the current converters have a pull configuration (the current direction is shown by arrows in *Figure 1-25*).

The adaptive functionality can be achieved by operation of transistor N in the linear region. With an average current increase (reflecting an increase in background), the V_{gs} values of the $P_1 \ldots P_k$ transistors are increased as well, which causes a reduction in the V_{ds} voltage of transistor N. The result is a fall in current at transistor N and a reduction of epsilon. Note that if a constant epsilon value is required, a stable current source (independent of the V_{sg} of $P_1 \ldots P_k$) can be used instead of transistor N.

Instead of using a transistor N, another simple option is to connect two parallel transistors, one with a relatively large W/L value operating in saturation and another with a small W/L operating in the linear region. This arrangement can achieve a constant epsilon by cutting off the transistor that is usually operated in the linear region and using only the saturation transistor. Alternatively, an adaptive epsilon value can be achieved by using the transistor operating in the linear region and cutting off the transistor that is in saturation.

In addition to background filtering, the circuit enables “no object” notification. If the control values of all pixels are “0”, the “no object” output is high and false alarms are reduced. However, noise levels vary with the background level and shot noise is higher at a higher background level. To achieve proper operation of the “no object” function, the minimum value of epsilon must therefore be limited.

The inputs to the WTA circuit depend on the filter control values — zero for a background pixel and pixel intensity level for an object pixel.

1.3.2.3.2 Elimination of bad pixels

Bad pixels can disrupt proper operation of the system. A bad pixel can have a high value, so it may be selected as the winner regardless of other pixel values. In the proposed CMOS smart tracking sensor system, bad pixels are disabled with a special "dark mode" in which a dark image is input. *Figure 1-26* shows the principal scheme for bad pixel elimination.

Bad pixels are eliminated in two stages. In the first stage (the dark mode), the *dark_mode* signal in *Figure 1-26* is "1" and the system processes a dark image — a very low background without an object of interest. The circuit finds bad bright pixels, using a regular WTA algorithm as described before. The frame must be scanned (processed) *N* times in order to find *N* bad pixels. After each additional frame scanning, a new bad pixel is found and its address is stored in the memory (using the *X_addr* and *Y_addr* buses in *Figure 1-26*).

In the second stage (regular system operation), the *dark_mode* signal is "0" and a real image is processed. For the "bad" pixels that were found in the dark mode stage, however, only ground values are transmitted to the filter and the WTA circuits. This is accomplished by comparing the address of every processed row (*in_addr* in *Figure 1-26*) with the *Y_addr* stored in the memory. If their values are equal, the comparator will output "1" and the *X_addr* of the bad pixel of this row is transferred to the *Dec. 6×64* block. In the array, the input bad pixel voltage is replaced with a ground value. The values of all bad pixels are replaced by ground, and thus bad pixels cannot be chosen as winners.

The fabricated prototype chip allows the elimination of up to three bad pixels. Adding more logic can easily increase this capacity.

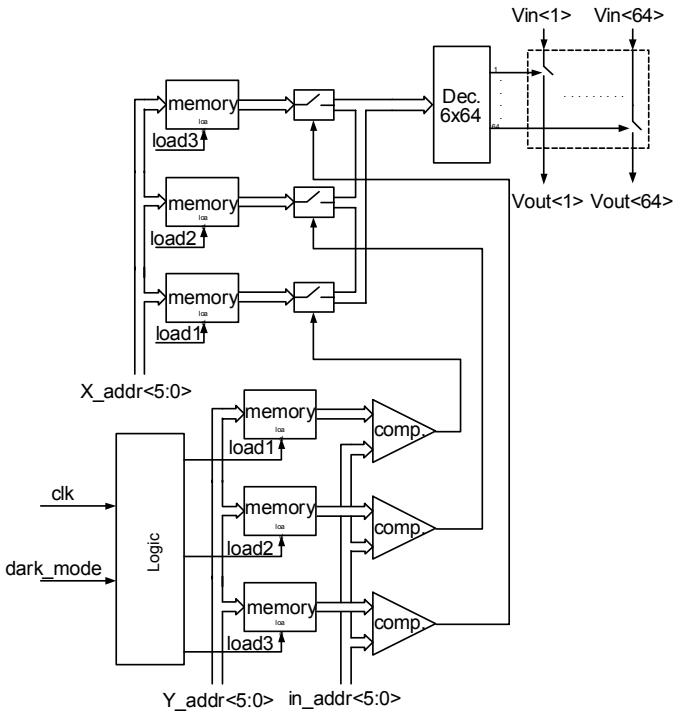


Figure 1-26. Principal scheme for bad pixel elimination in the CMOS smart tracking sensor.

1.3.2.4 Performance and test chip measurements

The CMOS smart tracking sensor system was designed and fabricated in a 0.5 µm, n-well, 3-metal, CMOS, HP technology process supported by MOSIS. The supply voltage was 3.3 V. A photograph of the test chip is shown in *Figure 1-27*. The test chip includes an APS array, row decoders, correlated double sampling circuit, an adaptive spatial filter, eight identical eight-input voltage WTA circuits, logic, a global winner selection circuit and a bad pixel elimination block.

The test chip was designed to allow separate modular testing of every functional block of the chip as well as measurements of the chip as a unit. The main separate blocks of the chip (the APS with CDS, the adaptive filter and the eight-input WTA circuit) were tested, as was the whole chip to check the functionality.

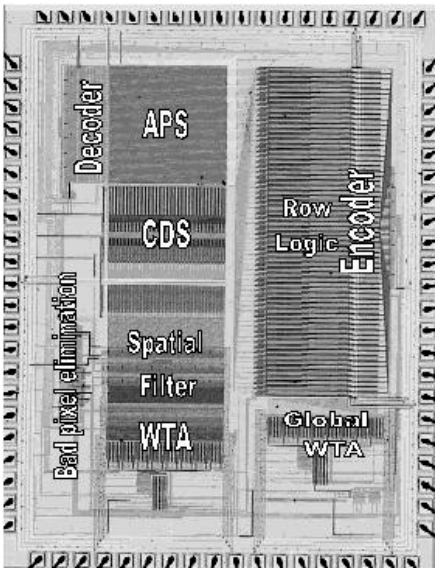


Figure 1-27. Photograph of the CMOS smart tracking sensor test chip.

1.3.2.4.1 APS with CDS

The layout of a single photodiode pixel of the CMOS smart tracking sensor is shown in *Figure 1-28*.

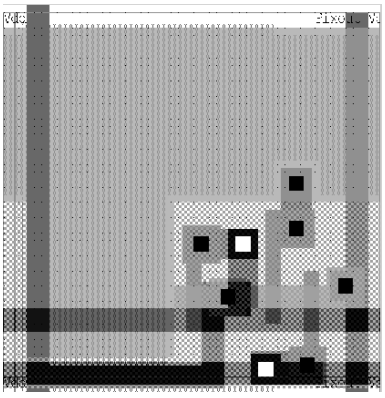
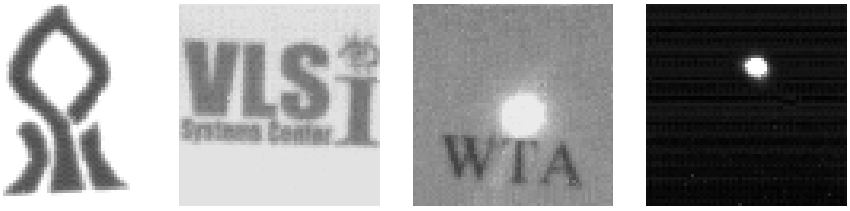


Figure 1-28. Layout of a single photodiode pixel of the CMOS smart tracking sensor.

As mentioned before, there is no penalty in spatial resolution for this architecture since the processing is done at the periphery. The pixel size is

14.4 µm × 14.4 µm and the fill factor is 49%. *Figure 1-29* shows four images as captured by the sensor under different background illumination levels.

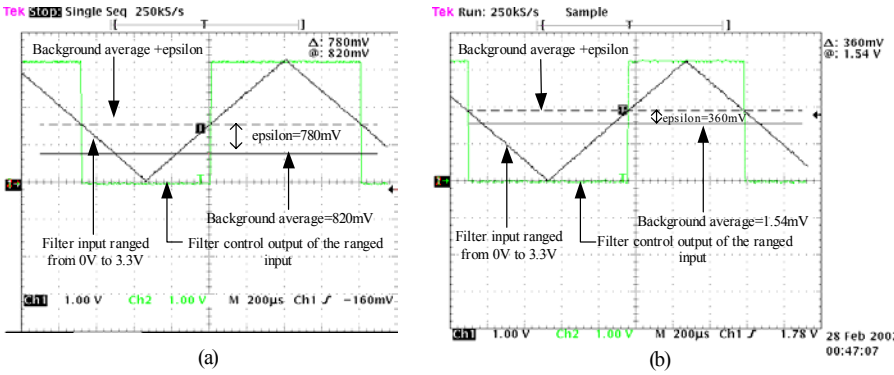


(a) (b) (c) (d)

Figure 1-29. Four images as captured by the APS: (a) the Ben-Gurion University logo on a high illumination background; (b) the VLSI Systems Center logo; (c) WTA with a laser beam spot; and (d) a laser beam spot on a dark background.

1.3.2.4.2 Adaptive filter measurements

Measurements were carried out at both low and high background levels to determine the properties of the filter. These measurements check the ability of the circuit to filter background regardless of its level and also check the dependence of the ε value on the background level. *Figure 1-30(a)* and *(b)* show the response of the filter to low and high backgrounds, respectively.



(a) (b)

Figure 1-30. Adaptive filter response for (a) a low background and (b) a high background.

In the first test, the average of the input voltages for a low background was 820 mV; this is represented by the horizontal solid line in *Figure 1-30(a)*. One of the filter inputs ranged from 0 V to 3.3 V; these inputs corresponded to the

background in the case of a low value and the object in the case of a high value. They are represented by the sloped sawtooth lines in *Figure 1-30*. The pulsed voltage in *Figure 1-30* is the filter control output (see *Figure 1-25*). This square wave is low for $V_{in3} < 1.6$ V and high for $V_{in3} > 1.6$ V. This value represents $V_{average} + \varepsilon$ when $V_{in3} = 1.6$ V. In this case, the ε value is 780 mV. As mentioned earlier, the ε value can be changed for this input vector by changing the *V*+ and *V*- control voltages.

The same procedure was performed to test the high background case, where the average was 1.54 V and the ε value was found to be 360 mV.

The filter responded as expected: a high epsilon value was generated for a low background level and a low epsilon value for a high background.

Figure 1-31 plots the epsilon value as function of background levels for different *V*+ values. As expected, an increase in *V*+ bias at a constant background level gives a higher epsilon value. On the other hand, the epsilon value decreases with background increase.

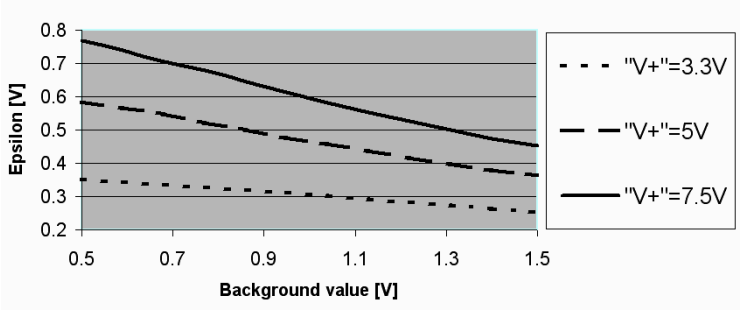


Figure 1-31. Epsilon value as function of background levels for different *V*+ values.

1.3.2.4.3 Measurements of the filter response and false alarm reduction

Figure 1-32 shows the filter response to four different images. The column beside each image shows the "no object" outputs for every row: white corresponds to "1" in "no object" output and black to "0". *Figure 1-32(a)* and *Figure 1-32(b)* present the same object of interest (a laser beam spot) but with two different background levels, a high background in *Figure 1-32(a)* and a low background in *Figure 1-32(b)*.

Because of the adaptive properties of the filter, the epsilon value is higher for the low backgrounds in *Figure 1-32(b)* and *(d)*, so the filtering is more aggressive and only very high values pass the filter. For the high backgrounds in *Figure 1-32(a)* and *(c)*, the epsilon value is lower and relatively lower

voltage values can pass the filter. The filtering process is thus more sensitive when a high background is present and the object input voltage is close to the background level. However, there is more freedom in filtering when a low background is present. In both cases, the object of the interest passes the filter. With a high background (small epsilon value), however, some pixels of the background succeed in passing the filter, while for a low background (high epsilon value) only the object pixels pass the filter. This effect can be seen in *Figure 1-32(a)* and *(b)*, where the "no object outputs" flags show the number of rows that succeed to pass the filter. As expected, *Figure 1-32(a)* has more "object" rows than *Figure 1-32(b)*. *Figure 1-32(c)* and *(d)* examine the false alarm reduction for low and high backgrounds. In both cases, the object of interest is not in the processed image and thus no signal passes the filter. The "no object" output is fixed on "1" when the object of interest disappears from the processed image, and therefore a false alarm is prevented for both levels of background.

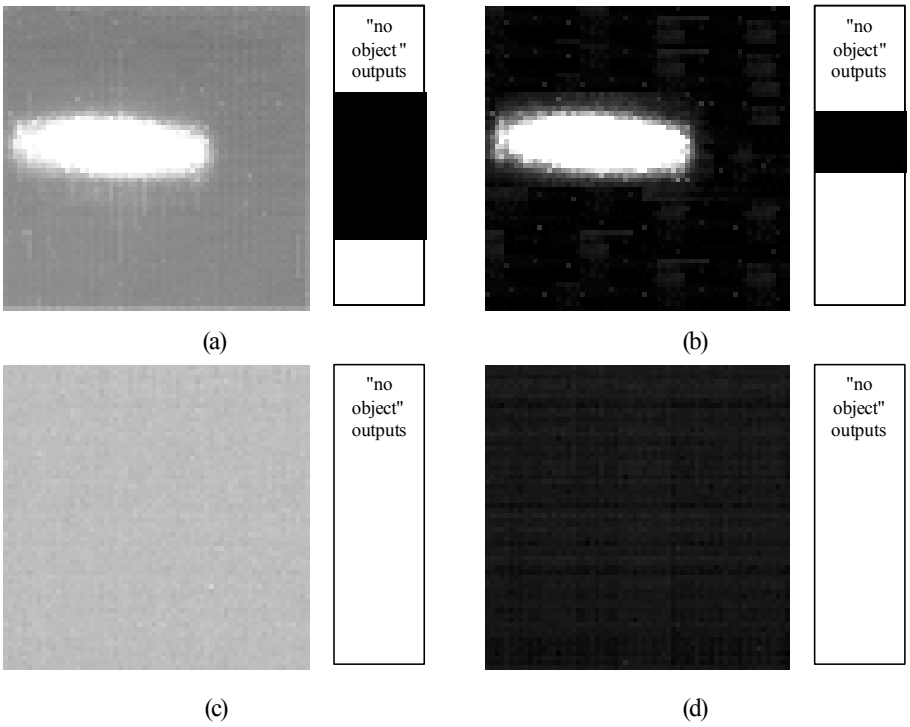


Figure 1-32. Adaptive filter response to four different images: (a) laser beam with a high background; (b) laser beam with a low background; (c) high background only; and (d) low background only.

1.3.2.4.4 The global winner measurements.

To examine the ability of the system to find the coordinates of the global winner, a focused laser beam was used as object of interest. *Figure 1-33(a)* shows the processed image; *Figure 1-33(b)* presents the winner as found by the system. As expected, the winner is the pixel farthest to the upper left in the first row of the object of interest.

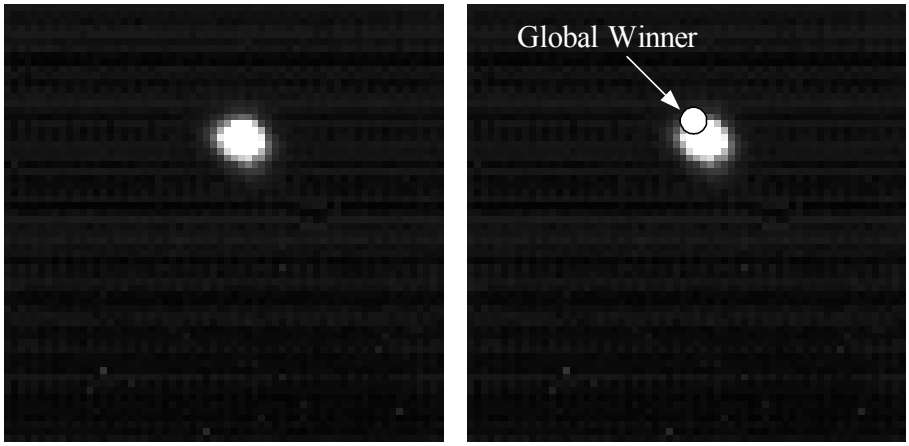


Figure 1-33. Global winner selection: (a) the processed image; and (b) the winner location.

Table 1-2 summarizes the chip specifications for the CMOS smart tracking sensor.

Table -2. Chip attributes for the CMOS smart tracking sensor.

Technology	HP 0.5 μm
Voltage supply	3.3 V
Array size	64 × 64
Pitch width	14.4 μm
Fill factor	49%
WTA mode	Voltage
WTA resolution	40 mV
Chip size (mm)	3.5 × 4.3
Frame scanning frequency	30 Hz
Minimum power dissipation (low background without object).	~28 mW
Typical power dissipation (the laser beam is ~10% of the frame)	~36 mW
FPN (APS)	0.15%
Conversion gain (APS)	7.03 μV/e^-
Dark response (APS output)	5.77 mV/s
Dynamic range	65 dB
Output voltage range	1.47 V

1.4 Summary

In this lecture, the area of CMOS imagers was briefly introduced. CMOS technologies, CCD technologies and different CMOS pixels were described and compared. The system-on-a-chip approach was presented, showing two design examples. The main advantages of CMOS imagers — low cost, low power requirements, fabrication in a standard CMOS process, low voltage and monolithic integration — rival those of traditional charge coupled devices. With the continuous progress of CMOS technologies, especially the decreasing minimum feature size, CMOS imagers are expected to penetrate into various fields such as machine vision, portable devices, security, biomedical and biometric areas, and other applications where custom sensors and smart pixels are required. More systems on chips will definitely be seen in the near future.

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