CCD versus CMOS – has CCD imaging come to an end?

NICOLAS BLANC, Zurich

ABSTRACT

CMOS image sensors are today challenging the existing Charge Coupled Devices (CCD) in several application fields. Improved architecture and processes have to a large extent overcome early weaknesses of CMOS imagers, namely with respect to noise and sensitivity. Todays “Active Pixel Sensors" are typically based on sub-micron technologies that have been optimized for optical sensing and can rival CCD in most aspects. In addition CMOS imagers offer significant advantages in terms of low power, low voltage and monolithic integration, allowing for example the manufacture of miniaturized single-chip digital cameras. The integration of added functionality on the chip or even at the pixel level also opens up completely new opportunities. This paper gives a short review of the advantages and weaknesses of both CMOS and CCD technologies for imaging applications.

1. INTRODUCTION

CCD technologies and image sensors have, since their discovery at the beginning of the seventies, evolved towards mature products which today can be found in almost all electronic image acquisition systems. More recently, alternatives based on standard CMOS technology have gained in turn considerable interest [1 - 4]. This is due on the one hand to the progress made on the technology side, with ever decreasing minimum device size, and on the other hand to several other key aspects such as the possibility to integrate analog and digital circuitry on-chip and the availability of low voltage, low power CMOS processes. The advances in solid-state technology allow today the production of optimized image sensors with additional functionality, tailored to a broad range of applications in optical metrology and machine vision.

Both CCD and CMOS image sensors are manufactured in a silicon foundry and the base materials (silicon, silicon oxide, polysilicon,..) and equipment used are similar. However CCD processes and imagers have been optimized specifically for imaging applications for more than 3 decades. They present today excellent performance and image quality, thanks to extremely low noise, low dark current, high quantum efficiency and fill factor. The main difference comes from the architecture and design flexibility of CMOS sensors especially for applications requiring dedicated signal or image processing that can be integrated on-chip, thus leading to a novel family of smart and compact imagers.

2. CCD

A CCD comprises photosites (either photodiodes or photogate) typically arranged in a 2D matrix of rows and columns. After exposure, each charge packet within the matrix is physically transported to a common output structure that converts the charge to a voltage. The architecture of CCD sensors thus leads to a sequential read-out of the image data with a high uniformity. Additional functions such as pixel - binning are often possible, offering lower spatial resolution at higher frame rate or with higher sensitivity.
Nevertheless, most CCDs still need clocking signals with relatively large amplitudes (5 – 10 Volts) and well defined shapes that are critical to their successful operation, requiring specialized clock drivers. Multiple supply and bias voltages at non-standard values are often necessary, adding to

system complexity and increased power consumption. It is worth noting that CCDs with lower clocking voltages (2.5 V) and power consumption (146 mW for a 1.3 Mega-pixel sensor @ 15 frames/s) have however recently been reported [5].

3. PASSIVE CMOS IMAGE SENSORS

Traditionally, “passive” CMOS image sensors contained in each individual pixel only a photo-sensing element (usually a photodiode) and a switching MOSFET, the signal being detected by an output amplifier implemented in each column or by a single output for the complete imaging device as depicted in Figure 1. These MOS-array sensors offer the advantage of random access to the individual pixels allowing the definition of sub-windows or "Regions Of Interest" (ROI) very useful for machine vision for example. The noise performance and sensitivity are however lower than those of CCD sensors, mainly due to large capacitances at the input of the output amplifier.

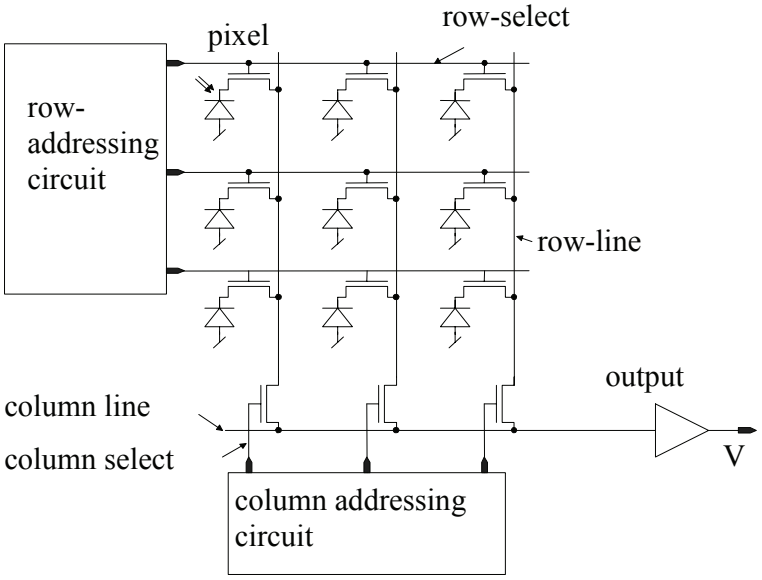

Figure 1. Architecture of CMOS passive image sensor [6]

4. ACTIVE PIXEL SENSORS

In Active Pixel Sensors (APS), the first amplification stage is implemented in every pixel (Fig. 2), improving the noise figures and thus the achievable dynamic range and S/N ratio [7]. Also in terms of spatial resolution and sensitivity (except for the lowest illumination levels or at higher temperatures) CMOS APS today present performance close to or better than their CCD equivalent: The largest CCD sensor has a resolution of 9216x9216 pixels [8], whereas the smallest pixels have a size of 2.4x2.4 μm. In comparison CMOS sensors with a resolution of up to 4096x4096 have been manufactured [9], while the smallest reported pixels have a size of 3.3 μm [10].

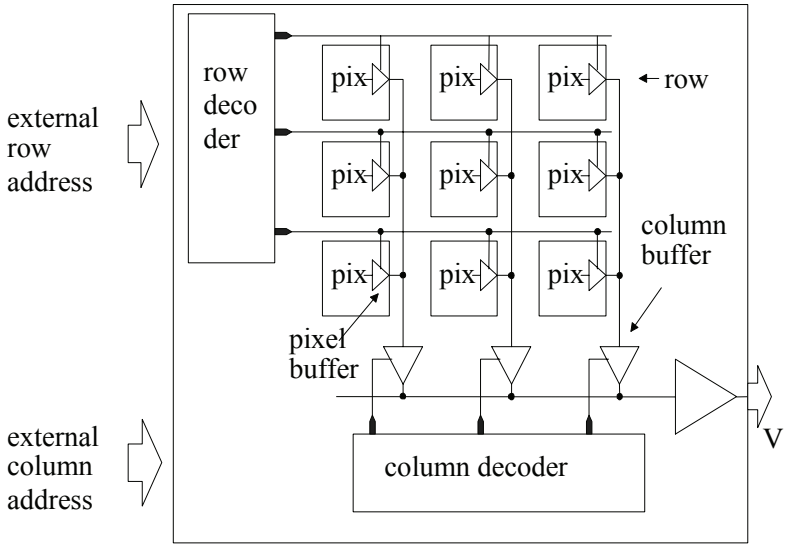

Figure 2. Architecture of CMOS Active Pixel Sensor (APS) [6]

Low-power single chip digital imagers

While CCD cameras require numerous chips for the sensor, drivers and signal conditioning, the use of standard CMOS mixed-signal technologies allows the manufacture of imaging devices that can be monolithically integrated: all the functions for timing, exposure control, ADC can be implemented on one single piece of silicon enabling the production of a complete camera on a single die. The reduced number of parts required has a positive impact on the overall reliability while decreasing system size and complexity. As an example, Figure 3 shows a miniaturized digital imager with a spatial resolution of 256x256 pixels, 10-bit ADC and featuring a single voltage supply of 3 Volts. The power consumption is 12 mW at the full speed of 60 images / s [11].

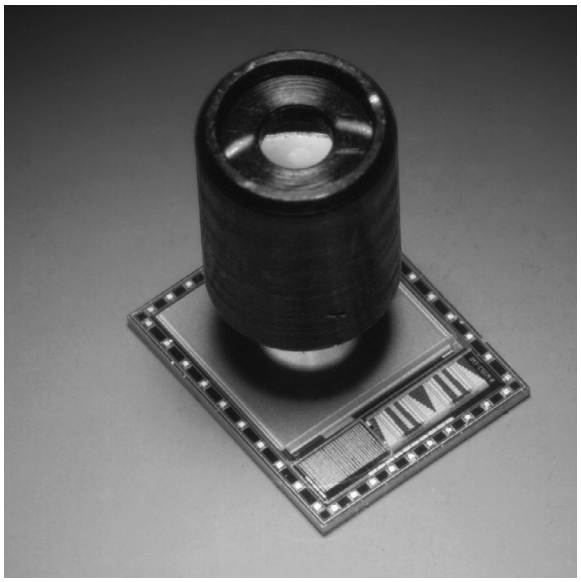

Figure 3. Digital single-chip imager (die size of 6.4x4.8mm2) with miniature optics [11]

CMOS digital imagers with consumption even as low as 550 μW for a QCIF digital imager @ 30 frames/s have been reported [12] opening new application fields such as portable devices (mobile phone, personal digital assistant).

Speed

Today's state-of-the art CMOS imagers continuously acquire about 1 Gigapixel / s thanks to the possibility of a massively parallel architecture and the integration of camera functions on the chip itself, reducing capacitances, inductances and thus propagation delays. Megapixel imagers (1024x768 pixels) can deliver up to 1000 frames/s at the full resolution using 32 analog outputs [13]. Similarly digital CMOS sensors with in pixel ADC have recently been developed in a 0.18 μm technology offering 10'000 frames/s at a resolution of 352 x 288 pixels [14].

Quantum efficiency and Fill Factor

The quantum efficiency (QE) is a measure of the ratio of collected electrons to incident photons. The QE of CCD and CMOS image sensors is mainly determined by the spectral response of the base material, silicon, with the thickness and doping levels used for the various layers. The other thin film materials involved in the process, mainly aluminum, polysilicon and the passivation layers, also have an impact on the QE. For CCD and CMOS imagers, the QE is typically excellent in the visible range (above 50% in the 400-700 nm). The QE in the UV range is limited by reflection and absorption in the top surface layers, in particular by the possible presence of polysilicon gates. Photodiode based sensors are superior in that respect. Polysilicon gates are typically used in Full Frame (FF) and Frame Transfer (FT) CCDs as well as photogate APS imagers, whereas photodiodes are implemented in many IT-CCDs and most CMOS APS imagers. The decreasing absorption coefficient of silicon in the IR range (essentially transparent above 1100 nm at room temperature) limits the sensitivity of silicon in the IR range. Antireflection coatings can be used to further increase the sensor responsivity. QE as high as 90% in the visible range has been achieved with back illuminated CCD as well as with CMOS imagers.

The fill factor, defined as the ratio of light-sensitive area to total pixel size, also determines the maximum achievable sensitivity. The fill factor of FF and FT CCDs is close to 100%, whereas this drops to about 30% for most IT-CCD and CMOS APS image sensors. With decreasing minimum feature size it becomes possible to increase the fill factor by keeping the pixel size not too small but decreasing the space used by the transistors found in each individual pixel. Microlens arrays or "Thin Film on ASIC" [15] allow further improvement in that figure, at the cost of additional processing.

Noise and dark current

Noise sources (i.e. random temporal noise and Fixed Pattern Noise, FPN) eventually limit the performance of image sensors. FPN is time-independent and arises from component mismatch due to process variations (lithography, doping levels, etc.). Calibration or appropriate electronics can effectively cancel out FPN. FPN correction can also be implemented on-chip using double sampling or correlated double sampling stages, so that carefully designed sensors should no longer suffer from FPN.
The temporal noise includes
1. dark current shot noise, from thermally generated charge carriers
2. and electronic noise (1/f noise, thermal noise and reset noise).

CCDs still have an advantage due to quieter sensor substrates and the use of common output amplifiers with larger geometries that can be adapted for optimal noise figures. Moreover standard CMOS image sensors suffer from higher dark currents (and hence dark current noise) of the order of 1 nA/cm2 at room temperature, often limiting their use to not too long exposure times. Several CMOS foundries are, fortunately, continuously optimizing their processes for imaging products with dark current of the order of 100 pA/cm2, to be compared to the 2-10 pA/cm2 for the best CCDs.

5. SMART SENSORS: 3D IMAGING

The ability to integrate dedicated signal processing capabilities or additional functions within the pixel site is finally the most significant difference between CMOS and CCD based imagers. In CMOS sensors the data processing can take place concurrently with the image acquisition.
A particularly interesting application example is the capability to realize new types of cameras for optical range imaging (i.e. the acquisition of 3D information). Range images are conventionally based on triangulation or interferometry. Another extremely powerful approach is derived from the Radar technology but in this case using a signal (an electromagnetic wave) in the visible or IR range of the electromagnetic spectrum. We have explored the capabilities and limitations of optical range imaging based on the time-of-flight (TOF) measurement of modulated light that is diffusely back-scattered by the objects in a scene [16]. The non-scanning TOF-camera is based on an array of "demodulation" pixels, where each pixel can measure both the background intensity and the individual arrival time of an RF-modulated scene illumination with an accuracy of a few hundreds of picoseconds. Thus both the target's distance and reflectivity can be determined simultaneously. The custom image sensors with patented lock-in pixels have been manufactured in a 2.0 μm CMOS process with a CCD option. The lock- imager is placed on a driver board, behind an array of LEDs that are modulated at frequencies up to 20 MHz. Depending on the application, either red (630 nm) or infrared (820 nm) LEDs have been used.

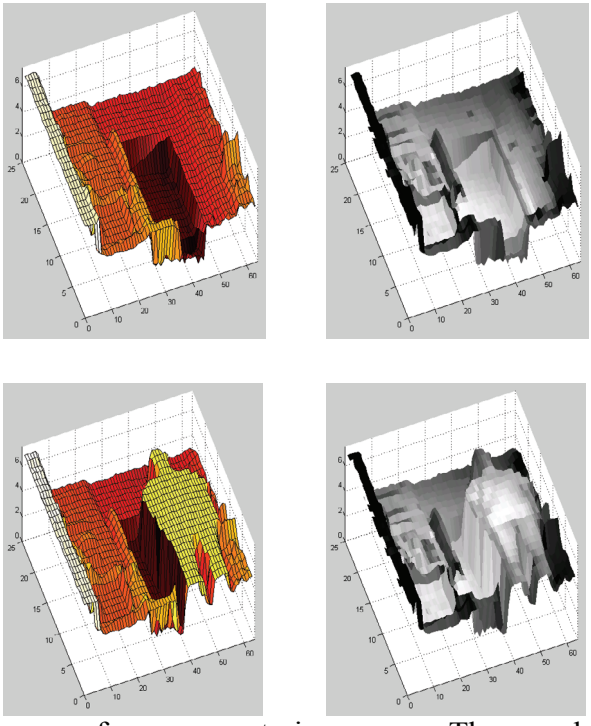

Figure 4: Range images of a person entering a room. The pseudo-3D range images (with 25x64 pixels) have a range resolution of around 4 cm. [17]

This first optical TOF camera without moving parts has confirmed that for a wide range of operation conditions its range resolution is limited only by the photon noise of the detected light. Range image sequences of scenes with non-cooperating objects, with a distance resolution of 3-10 cm over a measurement range of up to 20 m were successfully acquired. In Figure 4, examples of a few depth images acquired at a frame rate of 10 Hz are shown.

Two technological limitations currently prevent us from reaching a sub-centimeter distance resolution with the optical TOF range camera: The speed with which we can generate the digital timing signals and drive the CCD gates is limited today to about 20 MHz. Additionally, the long CCD gates due to the 2.0 μm technology employed lead to incomplete photocharge transport and reduced demodulation efficiency when working above 25 MHz modulation/demodulation frequencies. But the optical TOF range imaging technique will profit directly from the continuing improvements of the microelectronics industry, leading to electronic circuits that are faster, lower-power and smaller. Miniaturized, high-resolution optical TOF range cameras are expected to find many practical applications in safety, security, automotive, robotic and public transportation environments.

6. CONCLUSION AND OUTLOOK

CCD is still the technology of choice in high-end camcorders and digital still cameras, as well as science and astronomy. This supremacy is challenged by the novel developments in CMOS imagers. The latter are expected to penetrate into existing CCD markets, for example in machine vision, due to improved performances in terms of random access and speed as well as in the field of security / surveillance due to the higher integration / miniaturization. CMOS image sensors will be the technology of choice for new emerging markets, such as portable devices, consumer, biomedical, biometric and automotive, as well as applications that rely on custom sensors and smart pixels to locally extract the relevant information, such as the position, presence, distance or temperature of an object. But for the foreseeable future both technologies will remain to a large extend complementary.

7. REFERENCES

1. E.R. Fossum, "Active Pixel Sensors (APS) - Are CCDs Dinosaurs?", Proc. SPIE, Vol. 1900, 2-14 (1992).
2. D. Litwiller, “CCD vs. CMOS: Facts and Fiction”, Photonics Spectra, January 2001, 154-158
3. “CMOS vs. CCD and the Future of Imaging”, http://www.kodak.com/country/US/en/corp/researchDevelopment/technologyFeatures/cmos.shtml
4. A. Theuwissen, “Building a Better Mousetrap”, SPIE’s OE magazine, January 2001, 29-32
5. T. Yamada et al., “A 1/2 –in 1.3 M-Pixel Progressive-Scan IT-CCD for Digital Still Camera Applications”, IEEE Transactions on Electron Devices, Vol. 48, n°2, pp. 222-230, 2001
6. O. Vietze, “Active pixel image sensors with application specific performance based on standard silicon CMOS processes”, Thesis work, ETH Zurich N° 12038, Switzerland, 1997
7. P. Seitz, "Solid-State Image Sensing", in Handbook of Computer Vision and Applications (B. Jähne, H. Haussecker and P. Geissler, Eds.), Vol. 1, 165-222, Academic Press (2000).

8. “An ultra high resolution, electro-optical framing camera for reconnaissance and other applications using a 9216 by 9216 pixel, wafer scale, focal plane array”, SPIE Vol. 3431, p. 144, July 1998.
9. http://www.foveon.net/press_16megapix.html
10. D.-N. Yaung et al., “Non silicide Source/Drain Pixel for 0.25-μm CMOS Image Sensor”, IEEE Electron Device Letters, Vol. 22, n°2, pp. 71-73, 2001
11. N. Blanc et al., “Digital low-power camera on a chip”, International Workshop on Intelligent Communication Technologies and Applications, with Emphasis on Mobile Communications, May 5-7, 1999, Neuchâtel, Switzerland
12. Kwang-Bo Cho et al., “A Micropower Self-Clocked Camera-on-a-Chip” presented at the 2001 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, June 7-9, Cal-Neva Resort, Lake Tahoe, Nevada USA
13. S. Lauxtermann et al., “A mega-pixel high speed CMOS imager with sustainable Gigapixel/sec readout rate”, accepted for publication at the 2001 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, June 7-9, 2001, Cal-Neva Resort, Nevada 89402, USA
14. Stuart Kleinfelder et al., “A 10'000 Frames/s 0.18 mm CMOS Digital Pixel Sensor with Pixel-Level Memory”, presented at the 2001 International Solid State Circuits Conference, February 5, 2001
15. T. Lulé et al., “Sensitivity of CMOS Based Imagers and Scaling Perspectives”, IEEE Transactions on Electron Devices, vol47, n°11, Nov. 2000
16. R. Lange and P. Seitz, “Demodulation pixels in CCD and CMOS technology for TOF ranging”, Sensor Review, 20 (2000) 212.
17. R. Lange, Thesis work “3D Time-of-flight distance measurement with custom solid-state image sensors in CMOS/CCD-technology”, 2000