The Clock of STM32F4

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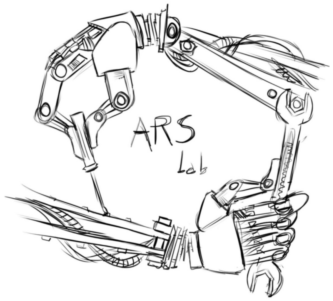

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STM32 and Clocks

- The STM32 has an internal **clock circuit** that has the objective of generating and distributing the clock signal for the CPU and all the peripherals
- The clock circuit is programmable, meaning that it can use different clock source and may apply division and multiplication factors
- Each family of STM32 MCUs has a different clock circuit with different features: here we consider the clock of STM32F4

STM32F4: Clock Types and Sources

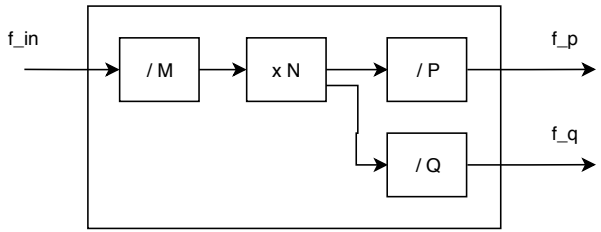
- The STM32F4 manages **two different** clock signals
  - **HS:** High Speed
  - **LS:** Low Speed
- Each clock signal is generated by **clock source** that can be:
  - **Internal:** Generated by a Resistor-Capacitor net
  - **External:** Generated by a quartz crystal resonator
- Therefore, we have the following signal names:
  - **HSI:** High Speed Internal
  - **HSE:** High Speed External
  - **LSI:** Low Speed Internal
  - **LSE:** Low Speed External

STM32F4: Clock Frequencies

- **Low Speed Clock** (LSI and LSE) must run at a fixed frequency of 32.768 *KHz*
- It is used to feed the **Real-Time Clock** circuit
- **HSI** (Internal High Speed) runs at a fixed frequency of 16 *MHz*
- **HSE** (External High Speed) can run at a frequency that goes from 4 *MHz* to 26 *MHz*

High Speed Clock: PLL

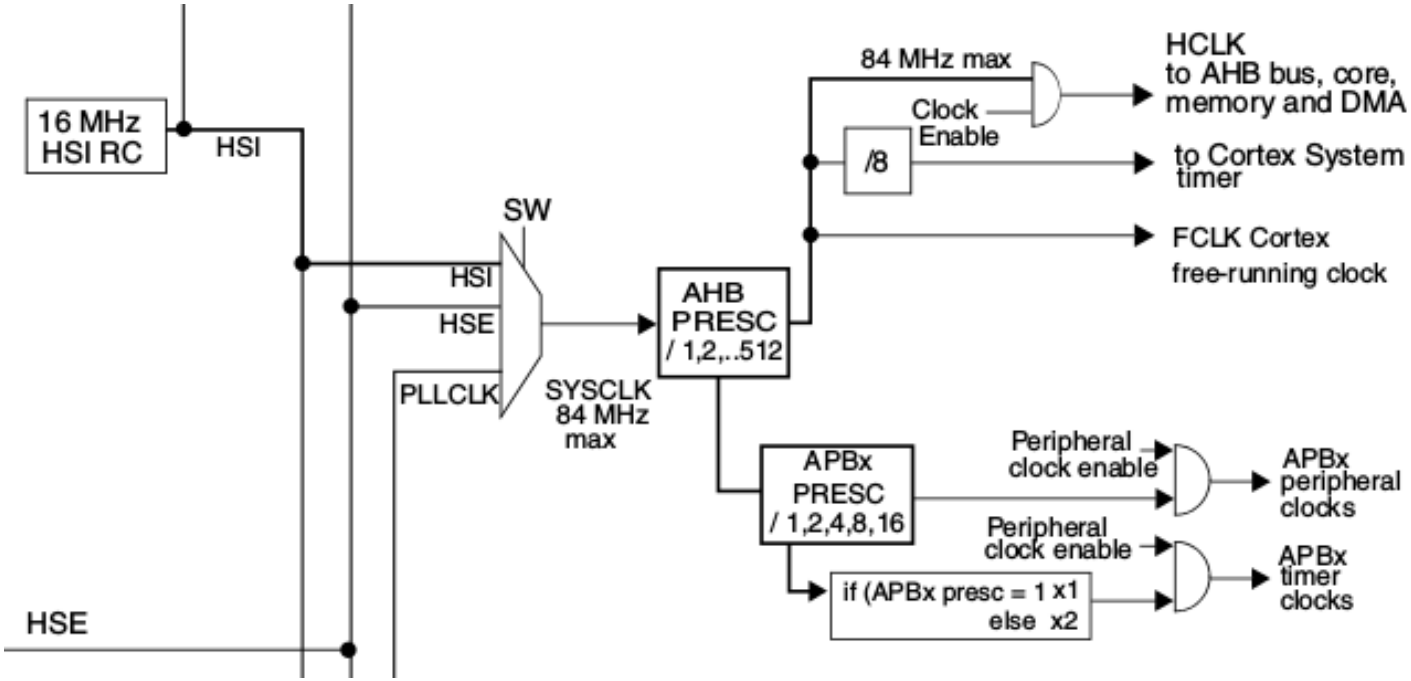
- The frequency of the HSI or HSE can be speed-up by using a circuit called **PLL = Phase Locked Loop**
- It is a standard circuit that can act as a frequency multiplier/divisor
- The PLL of the STM32 has two outputs and four factors N, M, P, Q



- $f_p = f_{in}\frac{N}{M \cdot P}$ $\quad$ $f_q = f_{in}\frac{N}{M \cdot Q}$
- f_q is the clock of USB and should be configured at 48 MHz

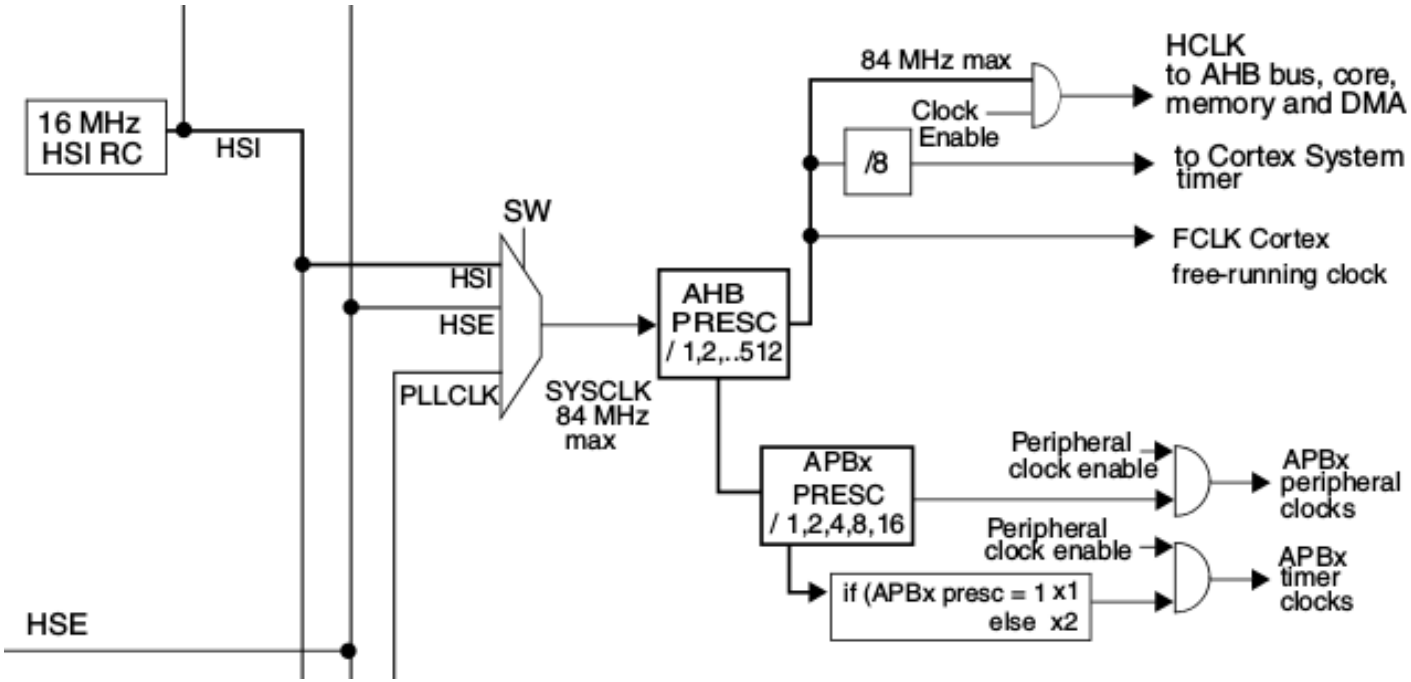
Clock Routing

- A multiplexer must be programmed to decide which kind of clock to send to CPU and peripherals:
  - **HSI**
  - **HSE**
  - **PLL**
- In STM32F4 the selected clock cannot exceed 84 *MHz*



Clock Routing and Busses

- The selected clock signal feeds three internal busses:
  - **AHB**, Advanced High-performace Bus, for CPU, Memory, DMA, GPIO
  - **APB1**, Advanced Peripheral Bus 1, some peripherals
  - **APB2**, Advanced Peripheral Bus 2, other peripherals
- Clock for APBx busses can be scaled by programming suitable prescalers



Clock Enable and Peripherals

- After having completed the configuration of clock circuit, the clock signal must be **enabled** for all peripherals used in our application
- There are **three enable registers**, each one for each bus
  - **AHBEN**
  - **APB1EN**
  - **APB2EN**
- In each register, each bit controls the enabling of a specific peripherals

AHB Clock Enable

- Advance High-performance Bus (AHB) controls the following hardware resources
  - **DMA**
  - **GPIO**
  - **CRC**

6.3.9 RCC AHB1 peripheral clock enable register (RCC_AHB1ENR)

Address offset: 0x30

Reset value: 0x0000 0000

Access: no wait state, word, half-word and byte access.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									DMA2EN	DMA1EN	Reserved				
									rw	rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			CRCEN	Reserved				GPIOHEN	Reserved		GPIOEEN	GPIODEN	GPIOCEN	GPIOBEN	GPIOAEN
			rw					rw			rw	rw	rw	rw	rw

APB1 Clock Enable

- Advance Peripheral Bus 1 (APB) controls the following hardware resources
  - **I2C**
  - **SPI**
  - **Timers**
  - **Watchdog**
  - **USART**

6.3.11 RCC APB1 peripheral clock enable register (RCC_APB1ENR)

Address offset: 0x40

Reset value: 0x0000 0000

Access: no wait state, word, half-word and byte access.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			PWR EN	Reserved				I2C3 EN	I2C2 EN	I2C1 EN	Reserved			USART2 EN	Reser-ved
			rw					rw	rw	rw				rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI3 EN	SPI2 EN	Reserved		WWDG EN	Reserved							TIM5 EN	TIM4 EN	TIM3 EN	TIM2 EN
rw	rw			rw								rw	rw	rw	rw

APB2 Clock Enable

- Advance Peripheral Bus 2 (APB) controls the following hardware resources
  - **SPI**
  - **Timers**
  - **ADC**
  - **USART**

6.3.12 RCC APB2 peripheral clock enable register (RCC_APB2ENR)

Address offset: 0x44

Reset value: 0x0000 0000

Access: no wait state, word, half-word and byte access.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TIM11 EN	TIM10 EN	TIM9 EN
													rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reser-ved	SYSCFG EN	SPI4EN	SPI1 EN	SDIO EN	Reserved		ADC1 EN	Reserved		USART6 EN	USART1 EN	Reserved			TIM1 EN
	rw	rw	rw	rw			rw			rw	rw				rw

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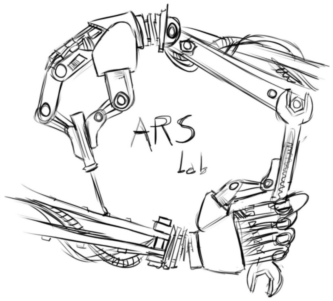

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