ASSEGNAZIONE $Rd = const$

OPERAZIONE TRA REGISTRI $Rd = Ra \ op \ Rb$

$op = +, -, *, /$

OPERAZIONE TRA REGISTRO E COSTANTE $Rd = Ra \ op \ cost$

ASSEGNAZIONE $Rd = const$

$dest\_REG = d$, $Const = const$

$nCONST\_ALU = 0$

OPERAZIONE TRA REGISTRI $Rd = Ra \ op \ Rb$

$op = +, -, *, /$

$Operand\_A = a$, $Operand\_B = b$

Operation =	op
00	+
01	-
10	*
11	/

$nREG\_const = 0$

$dest\_REG = d$

$nConst\_ALU = 1$

OPERAZIONE TRA REGISTRO E COSTANTE

$Rd = Ra$ op const

op = +, −, *, /

Operand_A = a , Const = const

Operation	op
00	+
01	−
10	*
11	/

nREG_const = 1

dest_REG = d

nConst_ALU = 1

ASSEMBLY

Rd = const	MOV Rd, #const
Rd = Ra + Rb	ADD Rd, Ra, Rb
Rd = Ra - Rb	SUB Rd, Ra, Rb
Rd = Ra * Rb	MUL Rd, Ra, Rb
Rd = Ra / Rb	DIV Rd, Ra, Rb
Rd = Ra + const	ADD Rd, Ra, #const
Rd = Ra - const	SUB Rd, Ra, #const
Rd = Ra * const	MUL Rd, Ra, #const
Rd = Ra / const	DIV Rd, Ra, #const

---

5 * 3 - 7 * 8

```
MOV R0, #5
MUL R0, R0, #3
MOV R1, #7
MUL R1, R1, #8
SUB R0, R0, R1
```

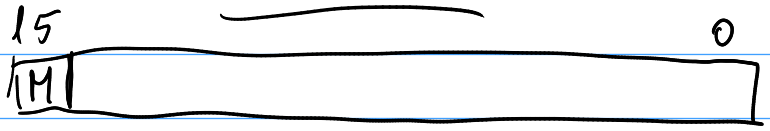
---

3 * (6 + 40) - 12 * 8

```
MOV R0, #6
ADD R0, R0, #40
MUL R0, R0, #3
MOV R1, #12
MUL R1, R1, #8
SUB R0, R0, R1
```

CODIFICA

16 bit

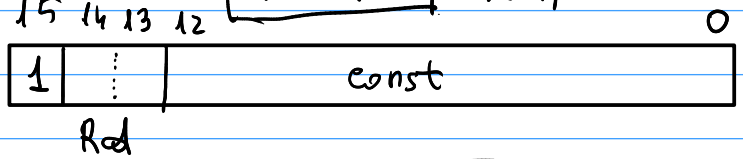


M = 1 MOV

M = 0 ADD, SUB, MUL, DIV

— ∘ —

MOV Rd, #const

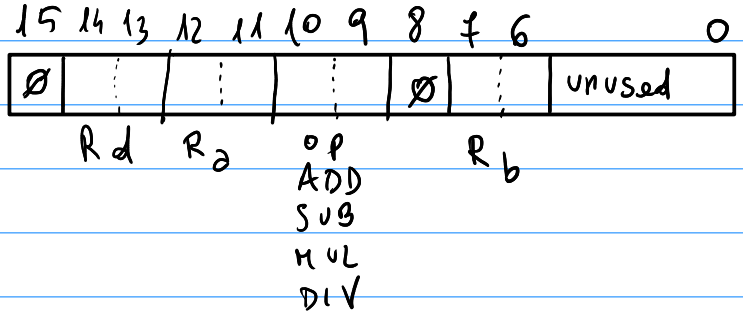


— ∘ —

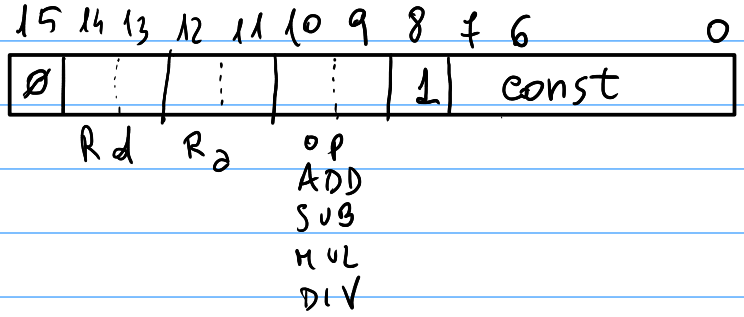
ADD, SUB, MUL, DIV

Rd, Ra, Rb

Rd, Ra, #const

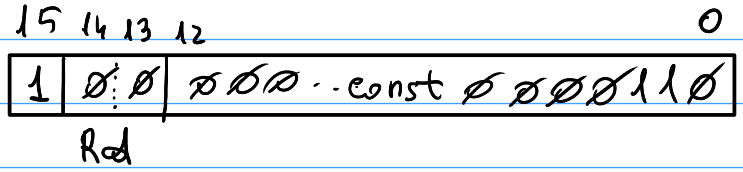


Rd, Ra, Rb

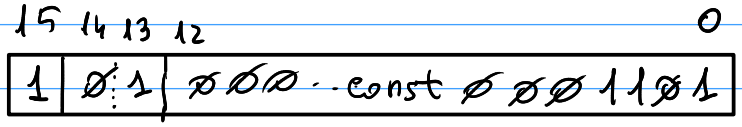


Rd, Ra, #const

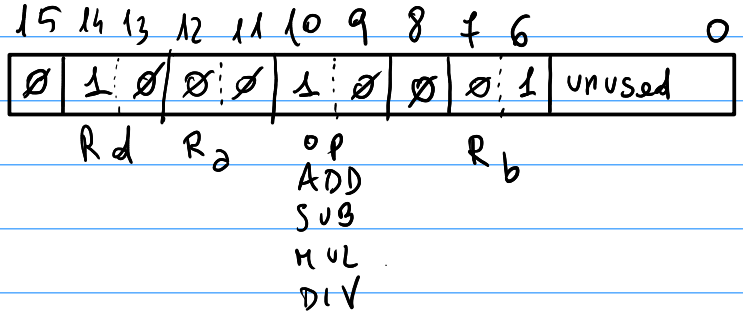
MOV R0 #6



MOV R1, #13



MUL R2, R0, R1



MUL R3, R1, #10