Porta Digitale di Input/Output

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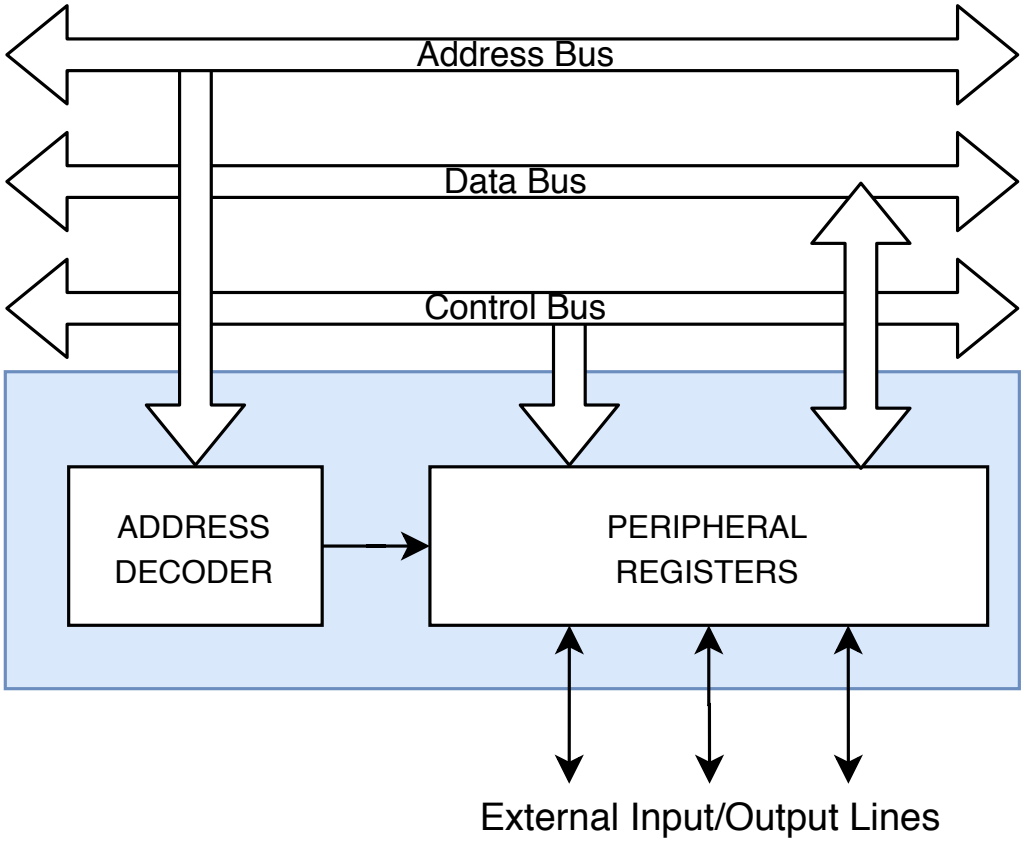
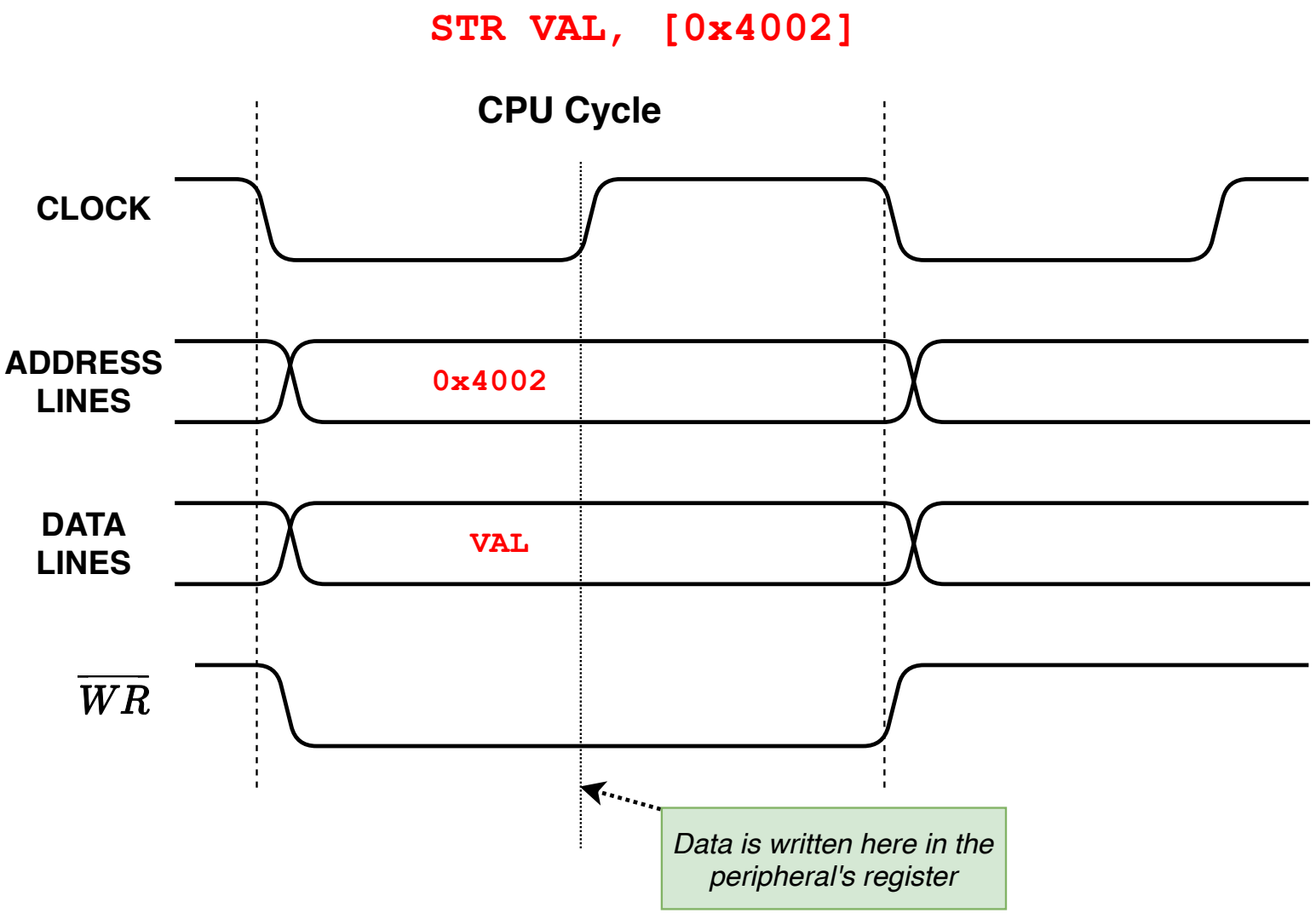
Architettura degli Elaboratori

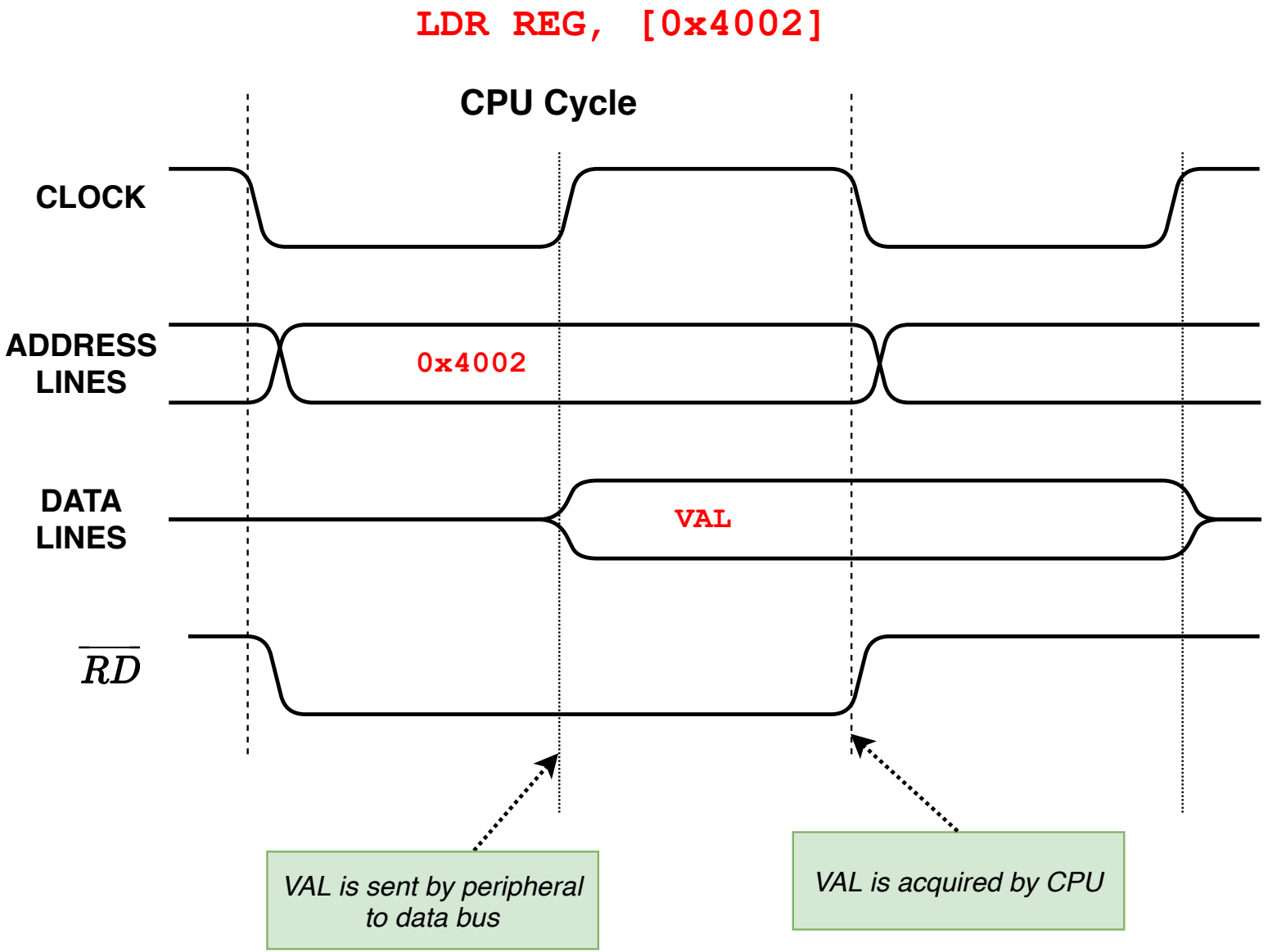
Bus di Sistema e Input/Output



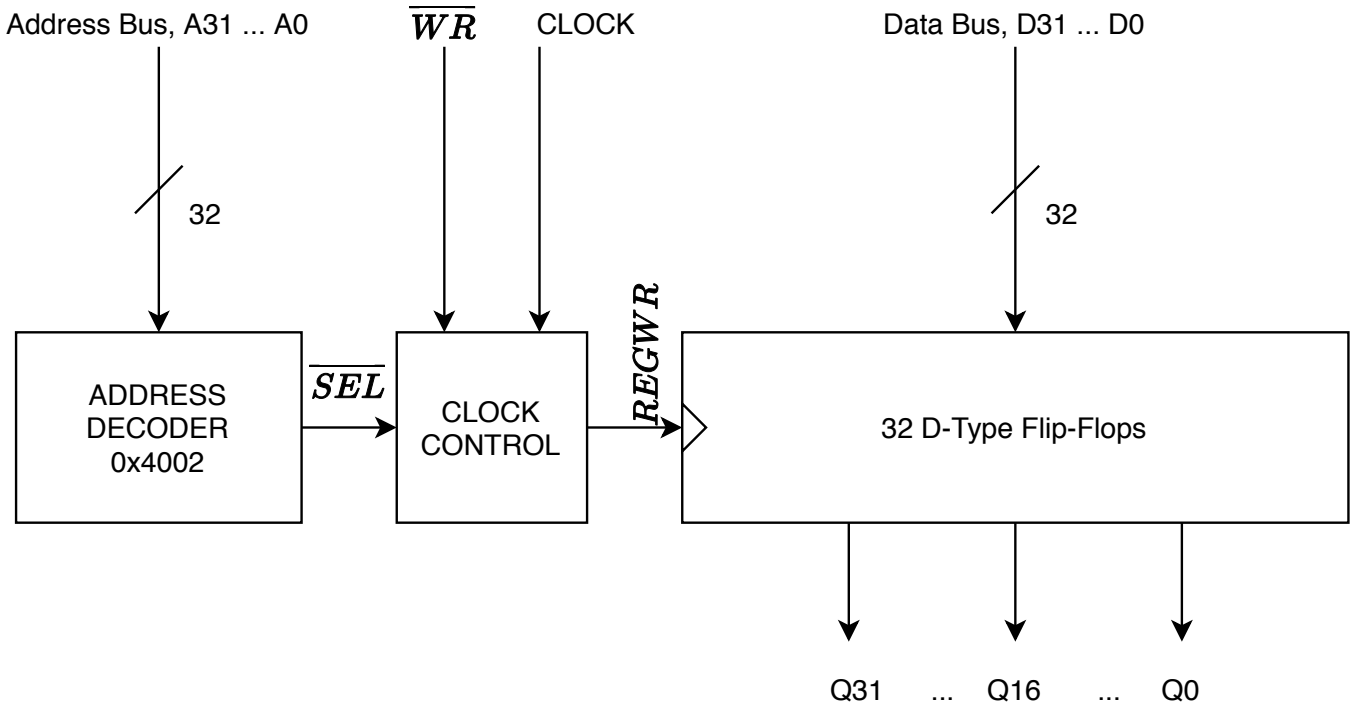
Bus Sincrono e Scrittura su I/O



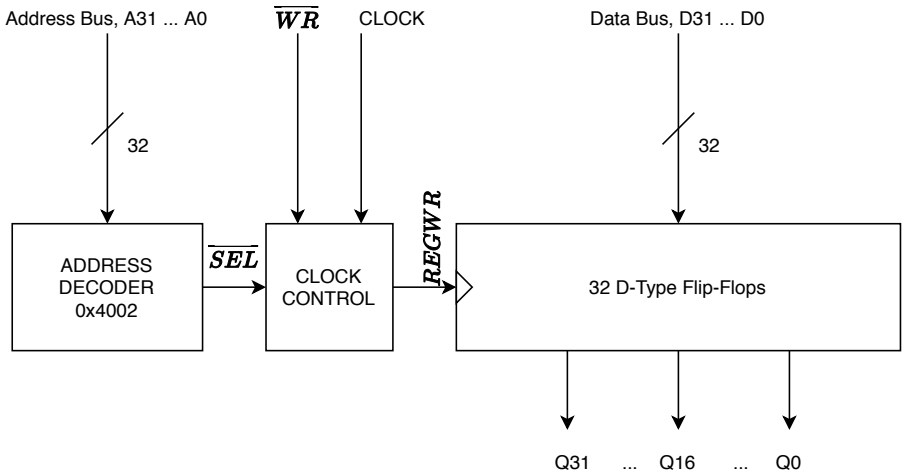
Bus Sincrono e Lettura da I/O



Esempio di Porta Digitale di Output



Esempio di Porta Digitale di Output

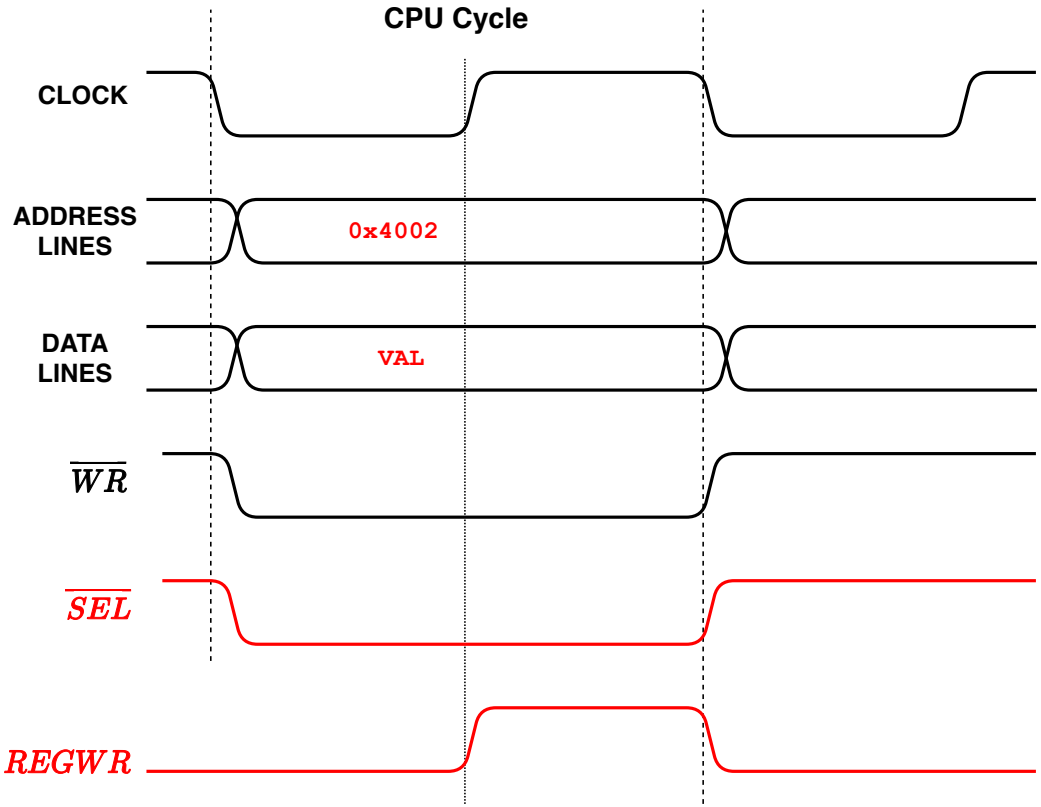


Address Decoder

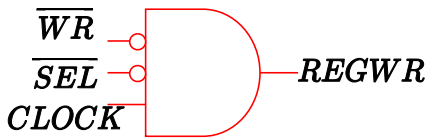
$$\overline{SEL} = 0, when \;\; address = 0x4002$$

$$\overline{SEL} = \overline{\overline{A_{31}} \ldots \overline{A_{15}} A_{14} \overline{A_{13}} \ldots \overline{A_3} A_2 A_1 \overline{A_0}}$$

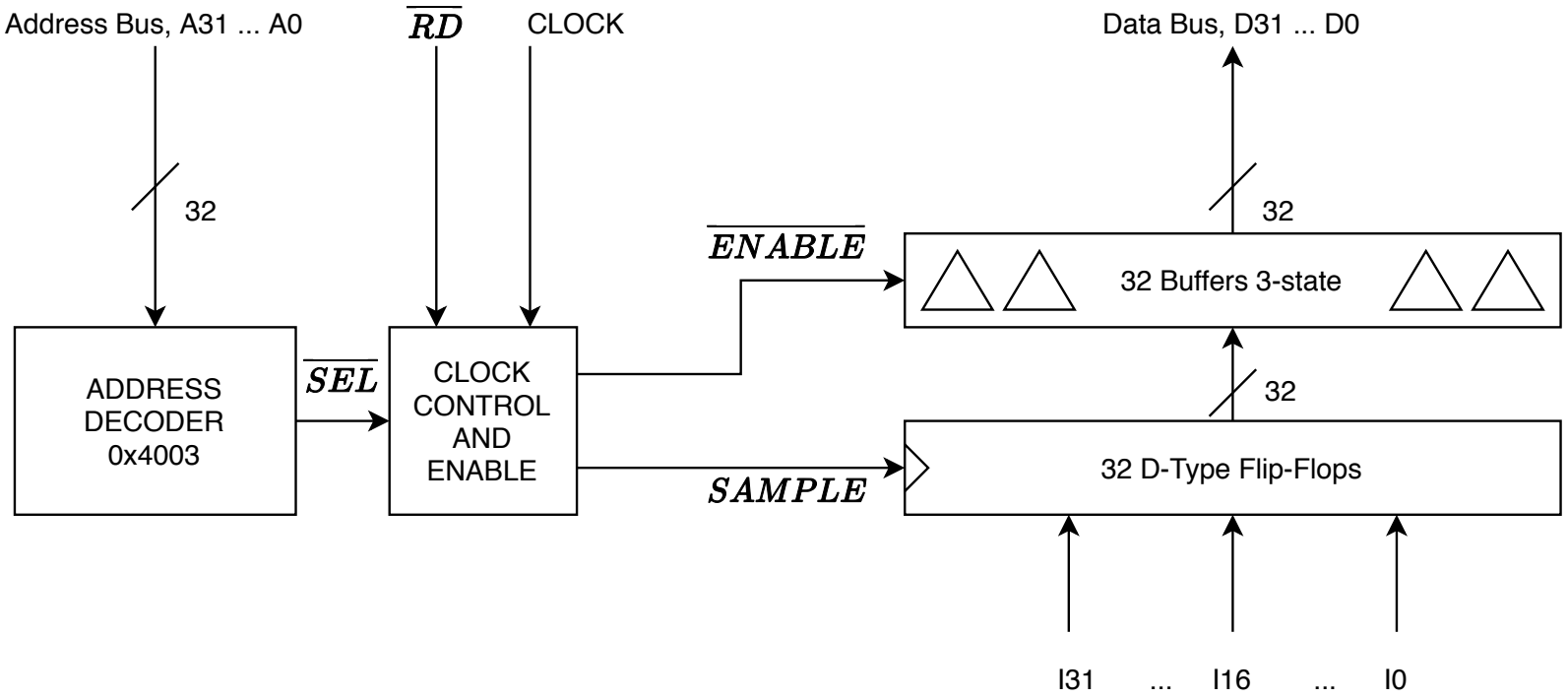
Esempio di Porta Digitale di Output



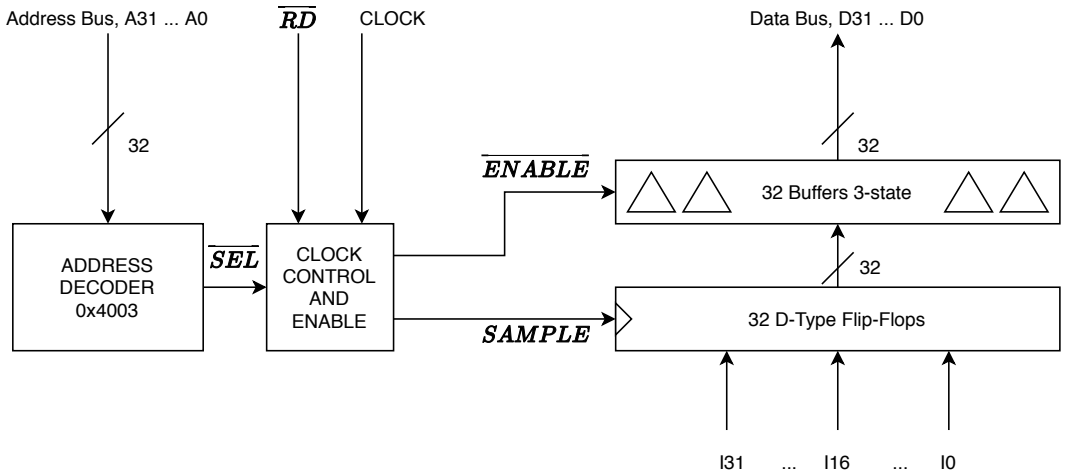
$$REGWR = CLOCK\ \overline{\overline{WR}}\ \overline{\overline{SEL}}$$



Esempio di Porta Digitale di Input



Esempio di Porta Digitale di Input

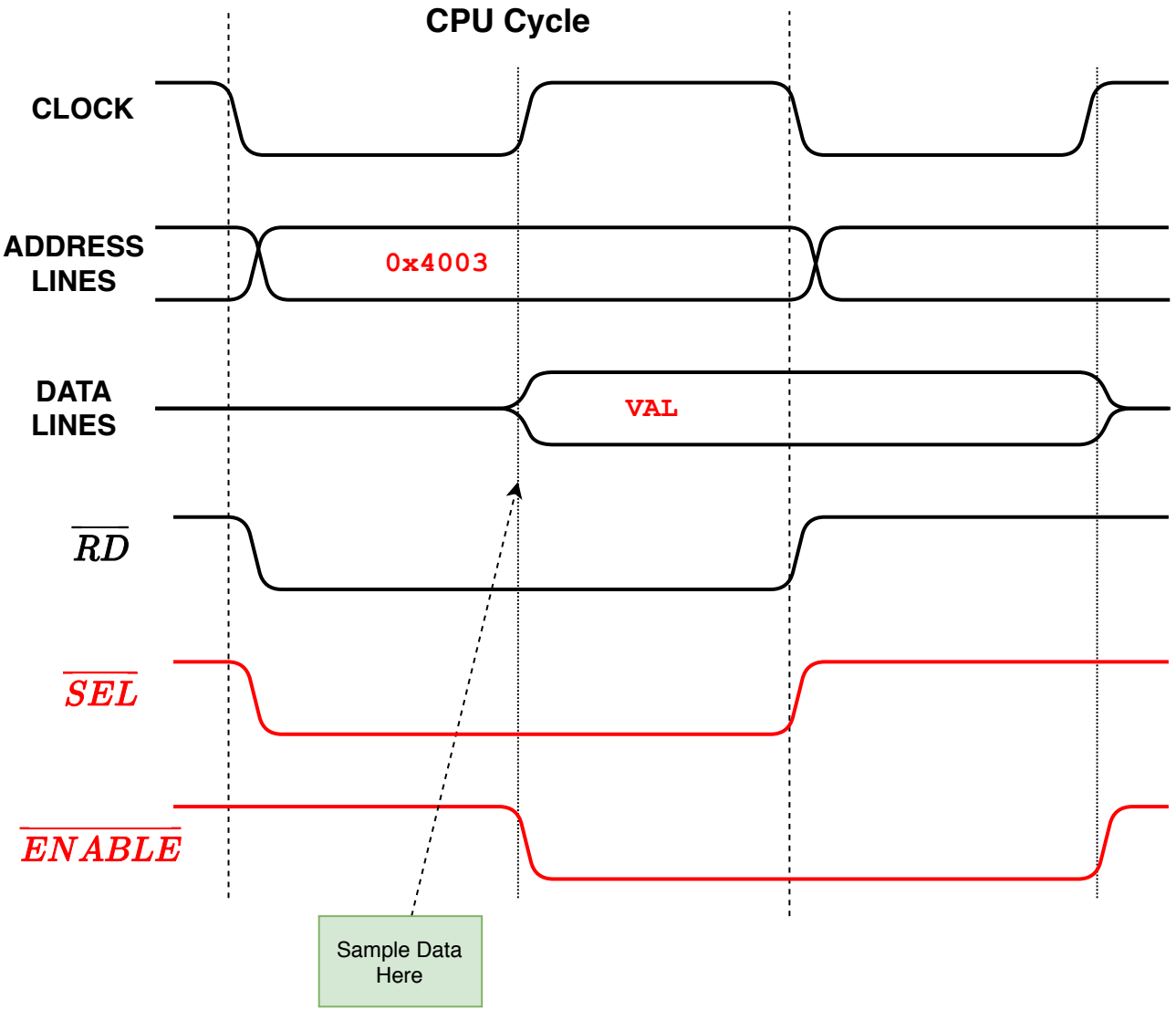


Address Decoder

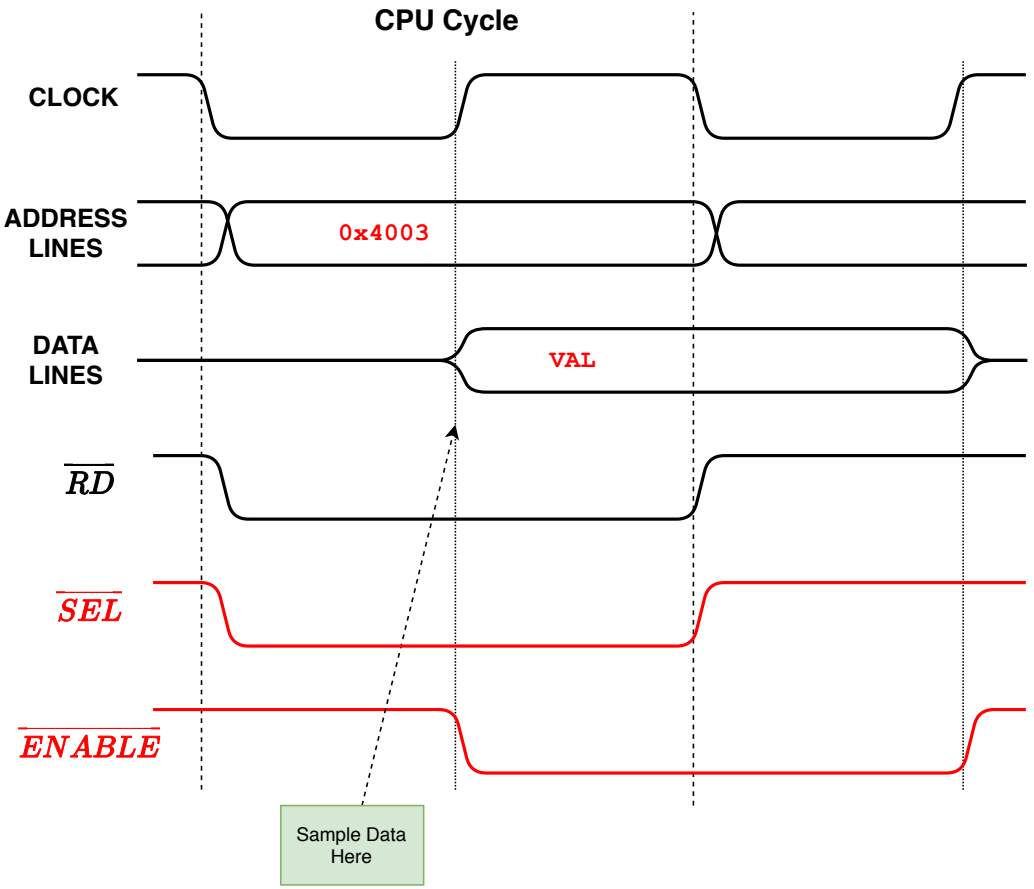
$$\overline{SEL} = 0, when \;\; address = 0x4003$$

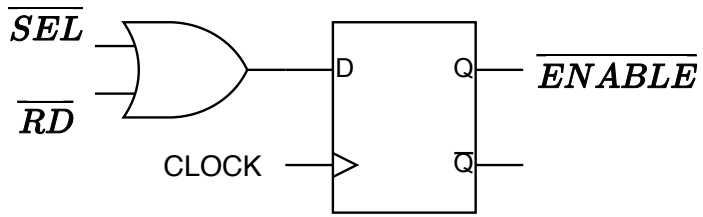
$$\overline{SEL} = \overline{\overline{A_{31}} \ldots \overline{A_{15}} \; A_{14} \; \overline{A_{13}} \ldots \overline{A_3} \; \overline{A_2} \; A_1 \; A_0}$$

Esempio di Porta Digitale di Input—Timing

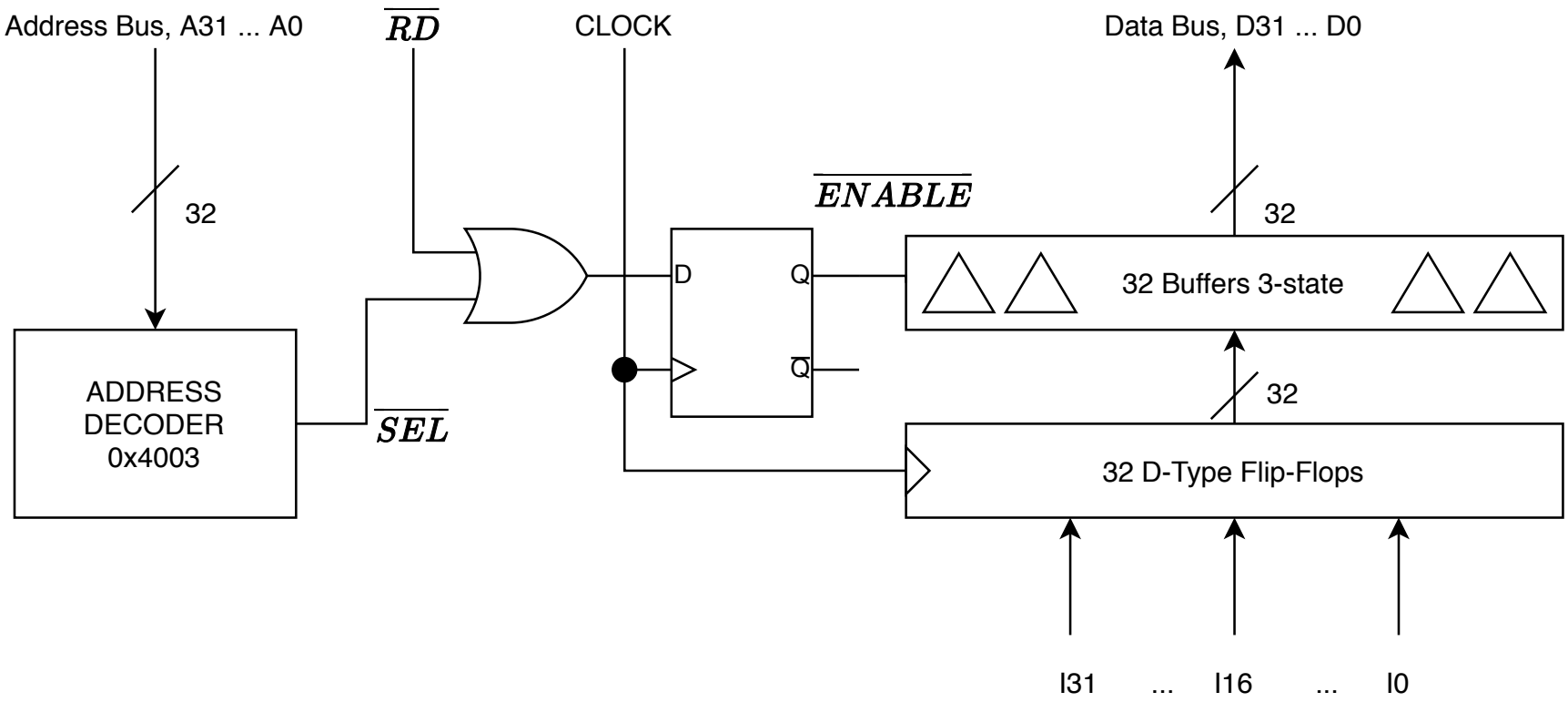


Esempio di Porta Digitale di Input—Segnale di Enable

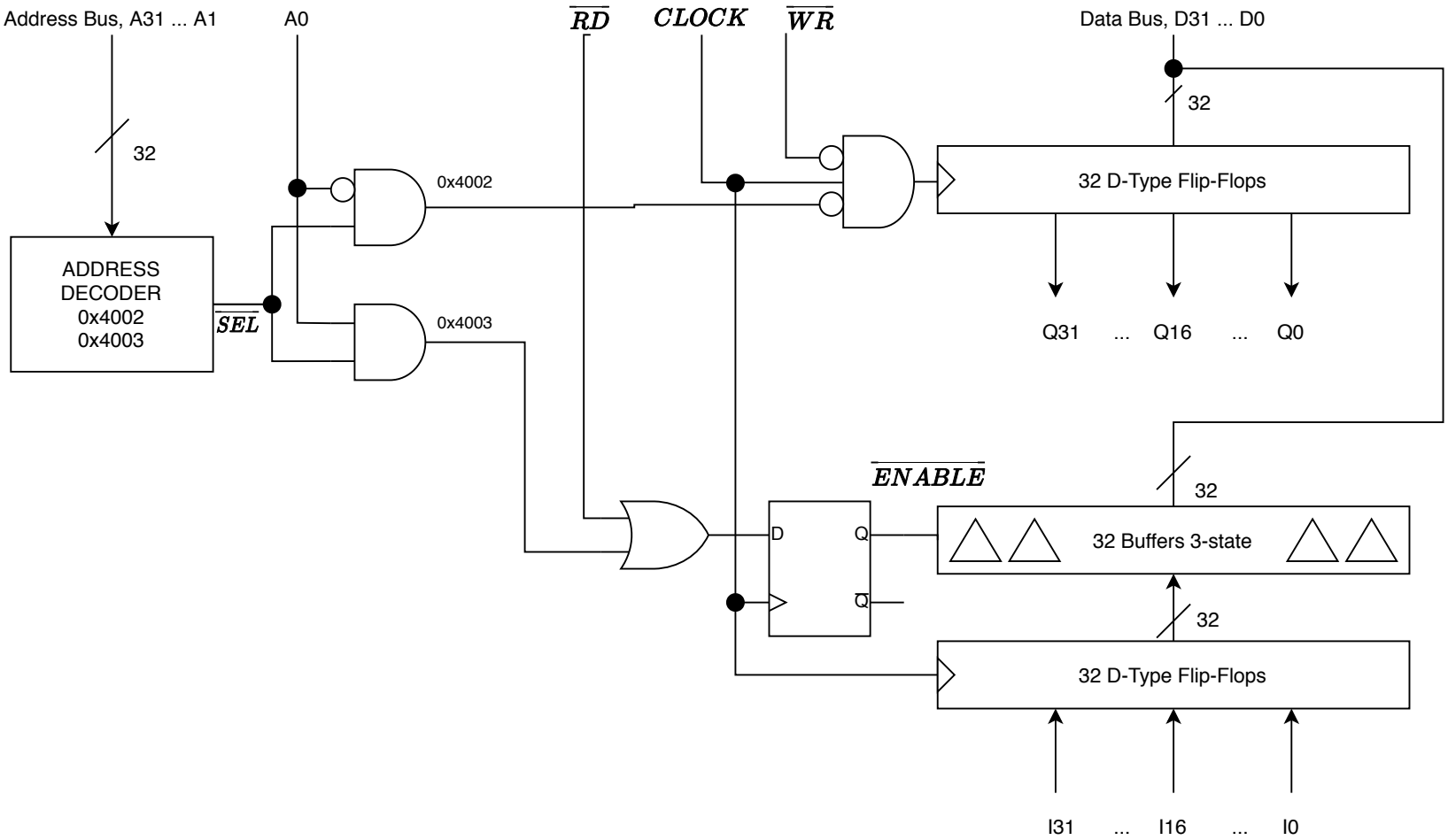




Esempio di Porta Digitale di Input



Porta Digitale di Input/Ouput Completa



$$\overline{SEL} = \overline{\overline{A_{31}} \ldots \overline{A_{15}}\ A_{14}\ \overline{A_{13}} \ldots \overline{A_3}\ \overline{A_2}\ A_1}$$

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