Component development on FPGA

Tutorial 09 on Dedicated systems

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Table of Contents

tutorial outline

this tutorial deals with:

- use of Qsys to design a hardware system including a Nios II processor
- integration and execution on FPGA of an application on a Nios II system designed with Qsys
- development of an Avalon memory-mapped component on FPGA

introduction to the Qsys software tool

development of a SoC with applications is a typical HW/SW codesign activity

> it consists of design and development of components of both kinds, as well as their *integration* to form a single system

the Quartus tool utilized in this lab tutorial for the integration of hardware components in SoC development is *Qsys*

> it enables one to select components such as processors, memories, I/O interfaces, timers, custom hardware components etc., in a GUI where their connections may be specified, and then to automatically generate the hardware description of the system

the subsequent compilation in Quartus produces a system for the programming of the FPGA, whereupon one may load a software application by means of the Monitor Program, compile it and execute it under control of the GDB debugger, as shown in the previous lab tutorial

in this lab tutorial two simple Qsys design cases are shown:

- construction of a Nios II system and execution of an application that handles two FPGA peripherals (switches and LED's)
- construction of a custom hardware component (a register) and its integration in a Nios II system through a memory-mapped slave interface on the Avalon bus, where its content is visualized on seven-segment displays

example of a Nios II system integration on FPGA

the first part of the classroom lab reproduces the execution of the example of Qsys construction of a Nios II system equipped with a small amount of on-chip memory and a couple of memory-mapped I/O peripherals with Avalon bus interfaces, as shown in the figure, described in the first reference tutorial

- the VHDL and software sources are available in the reserved lab area, as archive qsys_tutorial.zip, in folder VHDL/code/e09_classroom

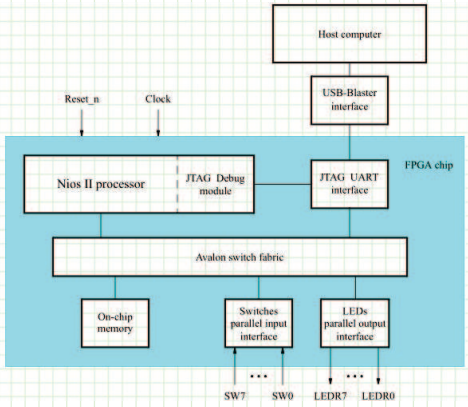

Figure 1. Block diagram of a simple example of Nios II system on FPGA

development of an Avalon memory-mapped component on FPGA

the second part of the classroom lab reproduces the execution of the example of construction of a Qsys system equipped with a memory-mapped custom hardware component with an Avalon bus interface, as shown in the figure, described in the second reference tutorial

- the VHDL sources are available in the reserved lab area, as archive component_tutorial.zip, in folder VHDL/code/e09_classroom

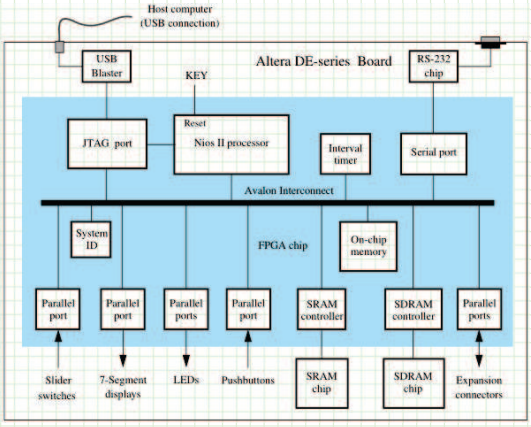

Figure 2. Block diagram of a complex example of Nios II system on FPGA

recommended readings:

Introduction to the Qsys System Integration Tool - *For Quartus Prime 16.1*, Intel Corp. - FPGA University Program, November 2016
Making Qsys Components - *For Quartus Prime 16.1*, Intel Corp. - FPGA University Program, November 2016