Component development on FPGA. Planning of student seminars

Tutorial 10 on Dedicated systems

Teacher: Giuseppe Scollo

University of Catania
Department of Mathematics and Computer Science
Graduate Course in Computer Science, 2017-18

Table of Contents

tutorial outline

this tutorial deals with:

- development of an Avalon memory-mapped component on FPGA
- planning of student seminars

development of an Avalon memory-mapped component on FPGA

the classroom lab reproduces the execution of the example of construction of a Qsys system equipped with a memory-mapped custom hardware component with an Avalon bus interface, as shown in the figure, described in the reference tutorial

the VHDL sources are available in the reserved lab area, folder VHDL/code/e10

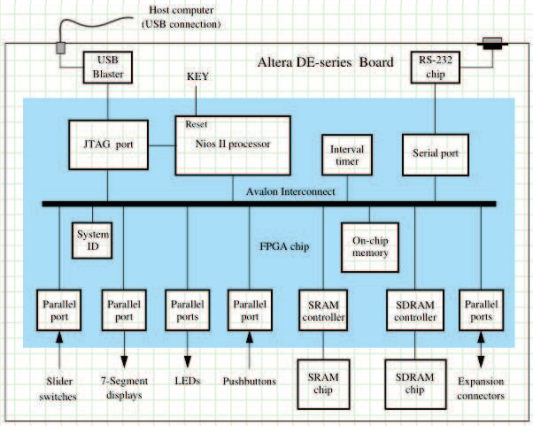

Figure 1. Block diagram of an example Qsys system implemented on and FPGA board

planning of student seminars

three options are proposed to the students:

- subject of (a part of) lecture 10
- subject of (a part of) lecture 11
- subject of lecture 12, with choice of specific application made by student according to own interest

after an overview of the reference materials, the first two options are chosen, with the following plan of the presentations by the students:

- lecture 10, part I, *Memory-mapped interfaces*, Grazia Pagano, monday 08/01/2018; reference material: Schaumont, Ch. 11, Sect. 11.1.1-11.1.5
- lecture 11, part I, *Functions, layout and design of hardware interfaces*, Salvatore Mameli, wednesday 10/01/2018; reference material: Schaumont, Ch. 12, Sect. 12.1-12.3.1

further references may be added by the students at a later time

references

recommended readings:

Making Qsys Components - For Quartus Prime 16.1, Intel Corp. - FPGA University Program, November 2016