

Quick learning guide

Dedicated systems

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Graduate Course in Computer Science, 2016-17

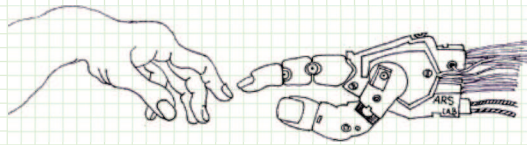


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Educational goals

To acquire and develop the following capabilities:

- model, design and optimal implementation of application-specific information processing systems
- use of hardware and software tools, such as development platforms for embedded systems, to design and to implement embedded systems for high-performance applications

Course organization

The course is organized in two modules: 24-hour lecture and 24-hour codesign lab (lecture room 24, on tuesdays and thursdays, 9-11 am)

Acquisition of the subject concepts and methods is supported by:

- attendance to lectures and problem solving
- participation to lab experiences
- study of reference readings
- consultation of supplementary readings
- experience with software tools and development platforms for embedded systems
- working out solutions to proposed problems and exercises, see **Test** area
- writing reports on lab experiences, in the same area
- interaction with teacher, weekly schedule:
 - G. Scollo: room 325 (I block, II floor) [phone]ext.: [095738]3007
 - on tuesdays and thursdays, 2:30-4:30 pm
- collaborative interaction with colleagues and teacher

Educational activities

Lectures: the study of the recommended readings sets the methodological grounds for effective application of a technology-transverse, result-unitary design approach:

versatile design of systems with optimal figure of merit that are dedicated to perform highly specialized tasks

Exercises: starting from a specification of the abstract functionalities of the system, the first problem which is often faced with is to select an architecture wherein to map them out, in order to further proceed to the synthesis of all components: hardware, software, communication interfaces. The proposed exercises deal with the different parts of this process.

Codesign lab: it is envisaged the use of development boards and platforms to implement embedded applications, ranging from on-board configuration to FPGA-based synthesis of components, up to System-on-chip (SoC) implementation. Reports on lab experiences may be outcomes of collaborative group work.

Seminars: as an experimental feature, some lectures (about 1/4 of the total) take the form of seminars that are prepared and delivered by students; one tutorial is devoted to the planning of the seminars. Critical evaluation of the educational activities is planned in the form of a written test that is part of the final exam.

Exams and evaluation

Oral exam, project (optional)

- evaluation objectives
- oral exam:
 - assessment of the achievement of educational goals
- optional project:
 - assessment of conceptual and scientific maturity exhibited in the practice of the subject
- oral colloquies
- assessment of critical learning of the subject
- evaluation of individual contribution to lab experience reports
- (optional) colloquy on individual use of subject concepts and methods within an original lab project, previously agreed with the teacher, that may be the outcome of a collaborative group effort
- exam schedule
 - first session: 7 february, 23 february
 - second session: 22 june, 11 july
 - third session: 12 september, 28 september
 - extra session: 11 april, 13 december

Exam success yields the acquisition of 6 credits.

Lecture Program

legenda: r = reference readings, s = supplementary readings, rn.# = reference lecture note, sn.# = supplementary lecture note #

1. Course goals and organization. Introduction to dedicated systems codesign
L01: 11/10/2016, r: S.01(1.1.4-1.4.1.1.6); s: VG.01(1.1-1.4)
2. Architectures and design process of dedicated systems
L02: 18/10/2016, r: S.01(1.1.2-1.1.3.1.5.1.7); s: VG.01(1.5-1.6), BF.01
3. Dataflow models, control flow
L03: 08/11/2016, r: S.02, s: L.S.06(6.3), M.02(2.5), sn.3, sn.4
4. Software implementations of dataflow models
L04: 15/11/2016, r: S.03(3.1), s: S.04
5. Synchronous systems as finite state machines with datapath (FSMD)
L05: 22/11/2016, r: S.05(5.3-5.4.3.5.6); s: S.05(5.7)
6. Microprogramming: architectures and control
L06: 29/11/2016, r: S.06(6.1-6.4); s: S.06(6.6-6.8)
7. Program design and analysis for dedicated systems
L07: 06/12/2016, r: S.07(7.1.7.3); s: S.07(7.2.7.5), sn.6
8. System-on-Chip (SoC) design
L08: 13/12/2016, r: S.08(8.1-8.3); s: S.08(8.4), R.01
9. Principles of HW/SW communication
L09: 20/12/2016, r: S.09(9.1-9.4)
10. Microprocessor interfaces
L10: 10/01/2017, r: S.11(11.1.1-11.1.5.11.2.0.11.3.0-11.3.1.11.3.3); s: S.11(11.1.6.11.2.1-11.2.2.11.3.2.11.3.4)
11. Hardware interfaces
L11: 17/01/2017, r: S.12(12.1-12.3.1.12.4); s: S.12(12.3.2)
12. Machine learning and FPGAs
L12: 24/01/2017, student seminar

Lab Tutorial Program

legenda: r = reference readings, s = supplementary readings, rn.# = reference lecture note, sn.# = supplementary lecture note #

1. Introduction to the combined use of Gezel with a VHDL simulator
E01: 13/10/2016, r: S.01(1.1.1), S.A(A.1), rn.1, rn.2; s: S.A(A.2)
2. Hardware description languages: Gezel, VHDL, Verilog, SystemC
E02: 20/10/2016, r: S.05(5.1-5.2), W.01, W.03-04; s: M.2(2.7), BF.aB, sn.1, sn.2
3. Introduction to design of hardware systems using FPGA
E03: 03/11/2016, r: W.02, W.05-06, rn.3, rn.4
4. Combinational and sequential network examples in VHDL
E04: 10/11/2016, r: W.20-21, W.24-25, W.27; s: Z.4(4.1-5), Z.6(6.1-5), rn.6(App.A)
5. Dataflow network examples in Gezel and in VHDL
E05: 17/11/2016, r: S.03(3.2)
6. FSMD examples in Gezel and in VHDL
E06: 24/11/2016, r: S.03(3.3), S.05(5.4.4-5.5), W.22
7. Microprocessor design example in VHDL
E07: 01/12/2016, r: S.06(6.5); s: W.08(8.1-8.3), Z.7(7.3-7.5)
8. Program analysis examples and use of instruction set simulators
E08: 15/12/2016, r: S.07(7.4.7.6.2); s: S.07(7.6.1.7.6.3), sn.5, sn.6, sn.7, sn.8
9. Planning of student seminars
E09: 20/12/2016
10. On-chip bus systems, SoC development with FPGA
E10: 12/01/2017, r: S.10(10.1), rn.5, rn.6; s: S.10(10.2-10.4)
11. Coprocessor and ASIP design on a SoC development board with FPGA
E11: 19/01/2017, r: rn.7, rn.8
12. Coprocessor design on FPGA for machine learning
E12: 26/01/2017, lab project

Recommended readings

Reference textbooks

N.B. The recommended parts are displayed in the lecture program, for each lecture, in the short form A.C(S), where: A = initials of textbook author(s), C = chapter, S = section(s)

P.R. Schaumont: *A Practical Introduction to Hardware/Software Codesign*
2nd Edition. Springer (2012)

with textbook corrections made starting from the 2013-2014 course edition

P. Wilson *Design Recipes for FPGAs: Using Verilog and VHDL*
2nd Edition. Newnes, Elsevier (2015)

Reference lecture notes

1. *Quartus II Introduction Using VHDL Designs* - For Quartus II 13.1, Altera University Program, April 2014
2. *Using TimeQuest Timing Analyzer* - For Quartus II 13.1, Altera University Program, 2014
3. *Quartus II Introduction Using Schematic Designs* - For Quartus II 13.1, Altera University Program, 2014
4. *Using Library Modules in VHDL Designs* - For Quartus II 13.1 Altera University Program, October 2013
5. *Introduction to the Altera Qsys System Integration Tool* - For Quartus Prime 16.0, Altera University Program, May 2016
6. *Making Qsys Components* - For Quartus Prime 16.0, Altera University Program, May 2016
7. *Using the SDRAM on Altera's DE1-SOC Board with VHDL Designs* - For Quartus Prime 16.0, Altera University Program, May 2016
8. *Nios II Custom Instruction User Guide*, UG-N2CSTNST, Altera Corp. (2015-11-02)

Supplementary readings

Textbooks

C. Brandolese, W. Fornaciari: *Sistemi embedded: sviluppo hardware e software per sistemi dedicati*
Pearson, Milano (2007)

E.A. Lee & S.A. Seshia: *Introduction to Embedded Systems - A Cyber-Physical Systems Approach*
2nd Ed., Version 2.0 (2015)

P. Marwedel: *Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems*
2nd Edition. Springer (2011)

C. Rowen: *iEngineering the Complex SOC - Fast, Flexible Design with Configurable Processors*
Prentice-Hall (2004)

F. Vahid & T. Givargis: *Embedded System Design: A Unified Hardware/Software Introduction*, Wiley (2002)

F. Vahid, T. Givargis & B. Miller: *Programming Embedded Systems: An Introduction to Time-Oriented Programming*
Version 4.0. Uniworld (2012)

M. Wolf: *Computers as components: Principles of embedded computing system design*
3rd Edition, Morgan Kaufmann (2012)

M. Zwolinski: *Digital System Design With VHDL*, 2nd Edition, Pearson (2004)

Supplementary lecture notes

1. F. Vahid (2006): Digital Design, Ch. 9, Hardware Description Languages (PDF slides)
2. D.J. Smith (1996): VHDL & Verilog Compared & Contrasted
3. Ghamarian et al. (2007): Latency minimization for Synchronous Data Flow Graphs
4. Stuijk et al. (2006): Exploring trade-offs in buffer requirements and throughput constraints for Synchronous Dataflow Graphs
5. *Introduction to the Altera Nios II Soft Processor*, Altera University Program, May 2016
6. *Introduction to the ARM® Processor Using Altera Toolchain*, Altera University Program, May 2016
7. *Altera Monitor Program Tutorial for Nios II*, Altera University Program, May 2016
8. *Altera Monitor Program Tutorial for ARM*, Altera University Program, May 2016

Lab activities consist of a series of experiences with the following topics:

- codesign and cosimulation in Gezel
- program optimization in C and assembly languages
- FPGA programming in VHDL
- codesign, simulation and performance evaluation on SoC development boards with FPGA

Forum, Moodle, Galileo: what goes where?

- Forum: discussions about
 - course organization, news, FAQ
 - problems with use of on-line services, software tools etc.
 - discussions about *ideas* of dedicated system projects
- Moodle (restricted access services):
 - access to educational support materials
 - development of proposed problems and exercises
 - discussions about topics relating to lectures, lab experiences and learning materials
 - group collaboration, delivery of lab experience reports
 - discovery and discussion of possible errors in learning materials (this may award *bonus points*!)
- Galileo:
 - development of dedicated systems projects
 - documentation and dissemination of results in the public domain