A Skill-Integrated Multi-Objective Optimization Tool for Analog Circuit Design

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STMicroelectronics
Outline

- Introduction
  - An IC optimization tool
  - Application to industrial benchmarks
    - 12-GHz Low Noise Amplifier
    - Leapfrog Filter
- Conclusions
Circuit design involves optimizing **multiple objectives** while satisfying several **constraints**

- Objectives: area, noise, speed, power, linearity,…
- Variables: transistor size, spiral inductor geometry, resistor/capacitor value,…

Very often two or more **objectives are conflicting**, thus tradeoffs could/must be investigated

Objectives and constraints are commonly defined in a **discrete domain** due to DFM issues
**Introduction**

- **Single-objective** optimization
  - searches maximum/minimum (optimal) solution(s)
  - gives no choice among different equally feasible (and optimal) solutions

- **Unconstrained** optimization is of limited applicability
  - problem re-formulation is necessary

- Techniques that do not manage **discrete** variables are useless in real-life problems
IC design is a multi-objective constrained optimization problem defined in a mixed continuous/discrete domain.

- size and complexity of the search domain makes **global optimization** mandatory.
- **random-based search** is exploited to:
  - avoid local minima trapping and preserve diversity
  - increase flexibility (no assumptions on continuity, differentiability, convexity, etc)
  - avoid the need for a good **initial guess**
Pareto dominance

- A dominates B if and only if:
  - all objectives of A are not worse than B
  - at least one objective of A is better than one of B

- Non-dominated solutions form the **Pareto set** (in the objective space is **Pareto front**)

- All points in the Pareto front are equally-good solutions in a multi-objective sense

- IC designer selects one point in the Pareto front on the base of his own considerations
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An IC optimization tool

Desired features

- Tightly integrated in the IC design environment
- Allows easy implementation of new algorithms
- Manages both scalars and vectors
- Performs parallel computation
- Allows for data post-processing
An IC optimization tool

Integration exploits the Skill Cadence language
An IC optimization tool

An IC optimization tool
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Application 1: 12-GHz LNA

Optimization variables (7)
- \( R_1 = R_2 = [100 : 100 : 10k] \)
- \( R_3 = [10 : 10 : 1k] \)
- \( C_{out}, C_3 = [10fF : 10fF : 1pF] \)
- \( Area_1, Area_4 = [1 : 1 : 10] \)
- \( V_{BE} = [800mV : 1mV : 900mV] \)

Objectives and constraints (2+3)
- \( I_C < 4 \, mA \)  \( \text{(minimize)} \)
- \( NF < 4.7 \, dB \)  \( \text{(minimize)} \)
- \( S_{11} < -14 \, dB \)
- \( S_{21} > 8 \, dB \)
- \( S_{22} < -6 \, dB \)
Application 1: 12-GHz LNA

2.0 2.2 2.4 2.6 2.8 3.0 3.2 3.4 3.6 3.8 4.0

4.3 4.4 4.5 4.6 4.7

Current [mA]

Noise figure [dB]

- 2 objs + 3 constr
- 3200 runs
- 1856 feasible points
- 519 non-dominated points

zig-zag due to discrete variables
Application 1: 12-GHz LNA

- 2 objs + 3 constr
- 7900 runs
- 4071 feasible points
- 1093 non-dominated points
Application 1: 12-GHz LNA

- **A** (yield = 64.5%)
- **B** (yield = 100%)
- **C** (yield = 48.5%)

Good probability of finding high-yielding points BEFORE design centering
### Application 1: 12-GHz LNA

<table>
<thead>
<tr>
<th></th>
<th>Objectives + constraints</th>
<th>First feasible point</th>
<th>Pareto/feasible/total run points</th>
<th>Yield*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-objective</td>
<td>2+3</td>
<td>180</td>
<td>519/1856/3200</td>
<td>100%</td>
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<tr>
<td>Multi-objective</td>
<td>2+3</td>
<td>180</td>
<td>1093/4071/7900</td>
<td>100%</td>
</tr>
<tr>
<td>Multi-objective</td>
<td>5+0</td>
<td>250</td>
<td>548/1397/4500</td>
<td>100%</td>
</tr>
<tr>
<td>Multi-objective</td>
<td>5+0</td>
<td>250</td>
<td>576/1918/8700</td>
<td>100%</td>
</tr>
<tr>
<td>Single-objective</td>
<td>0+5</td>
<td>470</td>
<td>86/450/2000</td>
<td>100%</td>
</tr>
</tbody>
</table>
Application 2: Leapfrog Filter

Objectives and constraints (3+13)
- GroupDelayRipple@9.1MHz < 20 ns
- GroupDelayRipple@9.7MHz < 40 ns
- GroupDelaySlope@6MHz < 3 fs/Hz
- PassBandGain > -0.01 dB
- InputNoise < 44 nV/Hz\(^{1/2}\) (minimize)
- PassBandRipple@9.1MHz < 0.8 dB
- PassBandRipple@9.7MHz < 1.8 dB
- StopBand@22.5MHz > 25 dB
- StopBand@34.2MHz > 56 dB
- DC current < 40 mA (minimize)
- OutputSwingOA1 < 2.8 V
- OutputSwingOA2 < 2.8 V
- OutputSwingOA3 < 2.8 V
- OutputSwingOA4 < 2.8 V
- InputResistance > 12.2 KOhm
- TotalArea < 18.000 um\(^2\) (minimize)

Optimization variables (20)
- \(C = [1fF : 1fF : 600fF]\)
- \(C_1 = [0.725n : 0.005n : 8.7n]\)
- \(L_2 = [18.625n : 0.01n : 223.5n]\)
- \(C_3 = [2.1n : 0.005n : 25.2n]\)
- \(L_4 = [11.875n : 0.01n : 142.5n]\)
- \(w_0 = [0.255 : 0.001 : 3.06]\)
- \(m_{1,2,3,4} = [0.01 : 0.01 : 60]\)
- \(k_{1,2,3,4} = [0.01 : 0.01 : 60]\)
- \(R_a = [1 : 0.005 : 12]\)
- \(\text{w}r_{p} = [14.125MHz : 0.005MHz : 169.5MHz]\)
- \(V_{n_{1,2,3,4}} = [5 : 0.05 : 60]\)
Application 2: Leapfrog Filter
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Pareto Front of Leapfrog Filter using 3 objectives, 13 constraints
Application 2: Leapfrog Filter
# Application 2: Leapfrog Filter

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<tr>
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<th>Error</th>
<th>First feasible point</th>
<th>Pareto/feasible/total run points</th>
<th>Yield*</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Multi-Objective</strong></td>
<td>3+13</td>
<td>0%</td>
<td>22500</td>
<td>2/2/23000</td>
<td>45.2%</td>
</tr>
<tr>
<td><strong>Multi-Objective</strong></td>
<td>3+13</td>
<td>0%</td>
<td>22500</td>
<td>75/199/36000</td>
<td>38.0% (best nom.) 69.4% (best yield)</td>
</tr>
<tr>
<td><strong>Single-Objective</strong></td>
<td>0+16</td>
<td>0%</td>
<td>26700</td>
<td>127/792/36000</td>
<td>7.0%</td>
</tr>
</tbody>
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- IC design is a multi-objective constrained optimization problem with mixed continuous/discrete variables.

- Integration in the IC design environment is mandatory to foster use within the designer community.

- Multi-objective optimization allows:
  - performance tradeoffs to be easily investigated
  - several equally feasible solutions
  - IC designers to make the final choice
Conclusions

A bilateral cooperation between STMicroelectronics and Cadence is being established
CDNLive! 2006
Nice, June 25-27 2006

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